KMRX10014M-B614

Samsung eMCP (embedded Multi-Chip Package) — 32 GB eMMC 5.1 + 4 GB LPDDR3

Manufacturer: Samsung Electronics Co., Ltd. **Category:** eMCP Memory (eMMC + LPDDR3) **Status:** Mass Production (Legacy)

1. GENERAL DESCRIPTION

The **KMRX10014M-B614** is a Samsung eMCP device that integrates **32 GB eMMC 5.1 NAND flash storage** and **4 GB (32 Gb) LPDDR3 mobile DRAM** into a single compact **221-ball FBGA** package. It is intended for smartphones, tablets, and space-constrained embedded systems, reducing PCB footprint while providing a complete memory subsystem.

The eMMC portion complies with the JEDEC eMMC Version 5.1 specification and supports HS200 / HS400 high-speed modes with up to 8-bit data bus width. The integrated LPDDR3 SDRAM operates at **1866 Mbps** (933 MHz). The device is identified by the product name **"RX14MB"** in the CID register.

Parameter	Value
NAND Storage Density	32 GB (eMMC 5.1)
DRAM Density	32 Gb (4 GB), LPDDR3
DRAM Data Rate	1866 Mbps (933 MHz)
Package	221-ball FBGA, 11.5 × 13.0 × 1.2 mm, 0.5 mm pitch
Operating Temperature	−25 °C to +85 °C

2. FEATURES

2.1 eMMC Subsystem

– JEDEC eMMC Version 5.1 compliant
– 32 GB user area (≈29.12 GiB usable)
– HS200 / HS400 high-speed interface modes
– Data bus width: 1-bit (default), 4-bit, 8-bit
– MMC interface clock: 0 – 200 MHz
– Boot clock frequency: 0 – 52 MHz
– Dual boot partitions (Boot1 / Boot2): 4 MiB each
– RPMB (Replay Protected Memory Block): 4 MiB
– General Purpose Partition support
– 64 MiB internal cache buffer
– Field Firmware Update (FFU) capable
– Hardware reset function (RST_n)
– Command queuing, Cache, Discard, Sanitize
– Secure write protection
– Embedded FTL: wear leveling, bad block management, ECC

2.2 LPDDR3 DRAM Subsystem

– 32 Gb (4 GB) LPDDR3 SDRAM density
– Maximum data rate: 1866 Mbps (933 MHz)
– Double-data-rate architecture
– Bidirectional differential data strobes (DQS_t / DQS_c)
– Differential clock inputs (CK_t / CK_c)
– 8 internal banks for concurrent operation
– Burst length: 8 (sequential)
– Auto precharge option per burst access
– Configurable drive strength
– All-bank / Per-bank / Self refresh
– Partial Array Self Refresh (PASR)
– Temperature Compensated Self Refresh (TCSR)
– Write leveling and CA calibration
– HSUL_12 compatible inputs

3. ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Storage Temperature	T_{STG}	−40	+125	°C
eMMC Core Supply (VCC)	V_{CC}	−0.3	+3.6	V
eMMC I/O Supply (VCCQ)	V_{CCQ}	−0.3	+3.6	V
LPDDR3 VDD1 Supply	V_{DD1}	−0.3	+2.0	V
LPDDR3 VDD2 / VDDQ Supply	V_{DD2}	−0.3	+2.0	V

DC Input Voltage (any pin)	V_{IN}	−0.3	V_{DDQ} + 0.3	V

CAUTION: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

4. RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Operating Temperature (Commercial)	T_C	−25	—	+85	°C
eMMC Core Voltage	V_{CC}	2.70	3.0 / 3.3	3.60	V
eMMC I/O Voltage (Signal Level 1)	V_{CCQ}	1.70	1.80	1.95	V
eMMC I/O Voltage (Signal Level 3)	V_{CCQ}	2.70	3.0 / 3.3	3.60	V
LPDDR3 VDD1 (Core / Logic)	V_{DD1}	1.70	1.80	1.95	V
LPDDR3 VDD2 (Array)	V_{DD2}	1.14	1.20	1.26	V
LPDDR3 VDDQ (I/O)	V_{DDQ}	1.14	1.20	1.26	V
LPDDR3 VDDCA (CA reference)	V_{DDCA}	1.14	1.20	1.26	V

5. ELECTRICAL CHARACTERISTICS

5.1 eMMC DC Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Input Low Voltage	V_{IL}	0	—	0.3 × V_{CCQ}	V
Input High Voltage	V_{IH}	0.7 × V_{CCQ}	—	V_{CCQ}	V
Output Low Voltage	V_{OL}	0	—	0.3	V
Output High Voltage (open-drain)	V_{OH}	V_{DD} − 0.2	—	—	V

5.2 eMMC AC Timing — HS400 Mode

Parameter	Symbol	Min	Max	Unit
Clock cycle time (data transfer mode)	t_{PERIOD}	5	—	ns
Slew rate	SR	—	1.125	V/ns
Clock duty cycle distortion	t_{CKDCD}	0	0.3	ns
Clock minimum pulse width	t_{CKMPW}	2.2	—	ns
Input data setup time	t_{SUddr}	0.4	—	ns
Input data hold time	t_{Hddr}	0.4	—	ns
Data strobe duty cycle distortion	t_{DSDCD}	0	0.2	ns
Data strobe minimum pulse width	t_{DSMPW}	2.0	—	ns

5.3 LPDDR3 AC Timing

Parameter	Symbol	Value	Unit
Data rate (per pin)	—	1866	Mbps
Array clock frequency	f_{CK}	933	MHz

Prefetch size	—	8n	—
Burst length	BL	8	words
Read latency (CAS latency)	CL	10 – 16 (configurable)	clocks
Write latency	WL	CL − 1 or CL − 2	clocks
Burst type	—	Sequential	—

6. DEVICE PARTITION INFORMATION

Partition	Size	Description
User Area	29.12 GiB (31,268,536,320 bytes)	Main user data storage region
Boot Partition 1	4 MiB	Primary boot code / bootloader
Boot Partition 2	4 MiB	Secondary / recovery bootloader
RPMB	4 MiB	Replay Protected Memory Block (authenticated access)
General Purpose Partitions (GP1 – GP4)	User-configurable	Optional enhanced user data areas

> **NOTE:** EXT_CSD Revision 1.8 (eMMC v5.1) | Access mode: sector mode | Default bus width: 8-bit (HS SDR 52 MHz during boot).

7. PACKAGE MECHANICAL INFORMATION

Parameter	Value	Unit
Package Type	221-ball Fine-Pitch BGA (FBGA)	—
Package Dimensions (L × W × H)	11.5 × 13.0 × 1.2	mm
Ball Pitch	0.5	mm
Total Ball Count	221	balls
Ball Composition	SAC305 (Sn-Ag-Cu) lead-free solder	—
Mounting Method	Surface-mount reflow soldering	—
Moisture Sensitivity Level	MSL 3	—
RoHS Compliance	Yes (lead-free / halogen-free)	—

8. DEVICE IDENTIFICATION REGISTERS

Register Field	Value	Note
Manufacturer ID (MID)	0x15	Samsung Electronics
Device / Product Name	RX14MB	ASCII: 0x525831344D42
Product Revision	0x00	Initial revision
Serial Number	0x6139AC23	Unique per device (sample value)
Manufacturing Date	July 2016	Encoded in CID as year / month
CID (full hex)	`15010052 5831344D 42006139 AC2373CC`	128-bit Card Identification register
CSD (full hex)	`D0270132 0F5903FF F6DBFFEF 8E40400C`	128-bit Card Specific Data register
Firmware Version	1.10	Dated 2017-03-26
Boot Version	1.04	—

9. ORDERING INFORMATION

Part Number	Description	Package	Status
KMRX10014M-B614	32 GB eMMC 5.1 + 32 Gb (4 GB) LPDDR3	221-FBGA, 11.5 × 13.0 × 1.2 mm	Mass Production (Legacy)

9.1 Part Number Decoding (Samsung eMCP Naming Convention)

Field	Code	Meaning
Family prefix	`KM`	Samsung MCP / eMCP memory family
eMMC density code	`R`	32 GB NAND density
Variant / generation	`X1`	Product variant and generation identifier
DRAM density	`0014`	32 Gb (4 GB) LPDDR3
Temperature grade	`M`	Commercial temperature grade
Package / speed code	`B614`	221-FBGA package, 1866 Mbps speed bin

10. TARGET APPLICATIONS

– Smartphones and feature phones (e.g. Samsung Galaxy C5 series)
– Tablets and phablet devices
– Portable media players and wearable devices
– IoT edge devices and smart home gateways
– Automotive infotainment systems (non-AEC-Q100 grade)
– Industrial control boards and HMI terminals
– Aftermarket repair and replacement service market

11. IMPORTANT NOTES

> **CAUTION — End-of-Life / Legacy Status:** This part has entered the end-of-life phase. Samsung has shifted production to newer LPDDR4X / LPDDR5-based uMCP solutions. Available inventory is sourced from channel stock, OEM surplus, and aftermarket suppliers. Verify authenticity before use.

> **CAUTION — Counterfeit Risk:** Due to the end-of-life status, refurbished, remarked, and counterfeit parts may exist in the supply chain. Always request date-code verification and supplier traceability documentation prior to procurement.