

TPS51200DRCR

Electronic Components Wholesale

IC-GOLDEN.COM

Overview of TPS51200DRCR

The **TPS51200DRCR** is a sink and source double data rate (DDR) termination regulator that is optimized for low input voltage, low-cost, low-noise systems with limited space. The TPS51200DRCR regulator comes in the thermally efficient SON-10 PowerPAD package and is Green and Pb-free. It has a temperature range of -40°C to +85°C.

TPS51200DRCR Key Features

1. Input Voltage: Supports 2.5-V Rail and 3.3-V Rail
2. VLDOIN Voltage Range: 1.1 V to 3.5 V
3. Sink and Source Termination Regulator Includes Droop Compensation
4. Requires Minimum Output Capacitance of 20- μ F (Typically 3×10 - μ F MLCCs)
for Memory Termination Applications (DDR)
5. PGOOD to Monitor Output Regulation
6. EN Input

TPS51200DRCR Key Features

7. REFIN Input Allows for Flexible Input Tracking Either Directly or Through Resistor Divider
8. Remote Sensing (VOSNS)
9. ± 10 -mA Buffered Reference (REFOUT)
10. Built-in Soft Start, UVLO, and OCL
11. Thermal Shutdown
12. Supports DDR, DDR2, DDR3, DDR3L, Low Power DDR3, and DDR4 VTT Applications
13. 10-Pin VSON Package With Thermal Pad

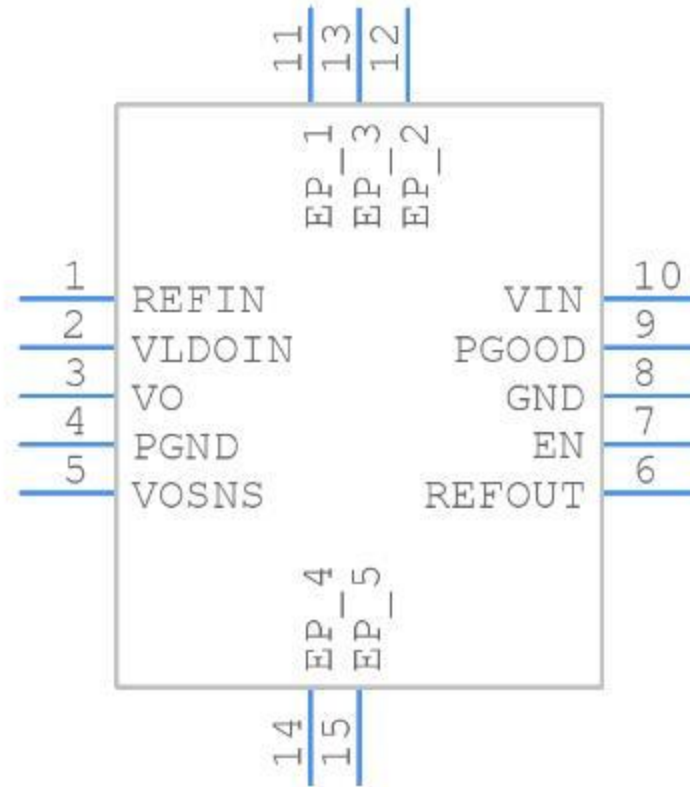
TPS51200DRCR Applications

1. Memory Termination Regulator for DDR, DDR2,
2. DDR3, DDR3L, Low-Power DDR3, and DDR4
3. Notebooks, Desktops, and Servers
4. Telecom and Datacom
5. Copiers and Printers
6. Set-Top Boxes
7. Base Stations
8. LCD-TVs and PDP-TVs

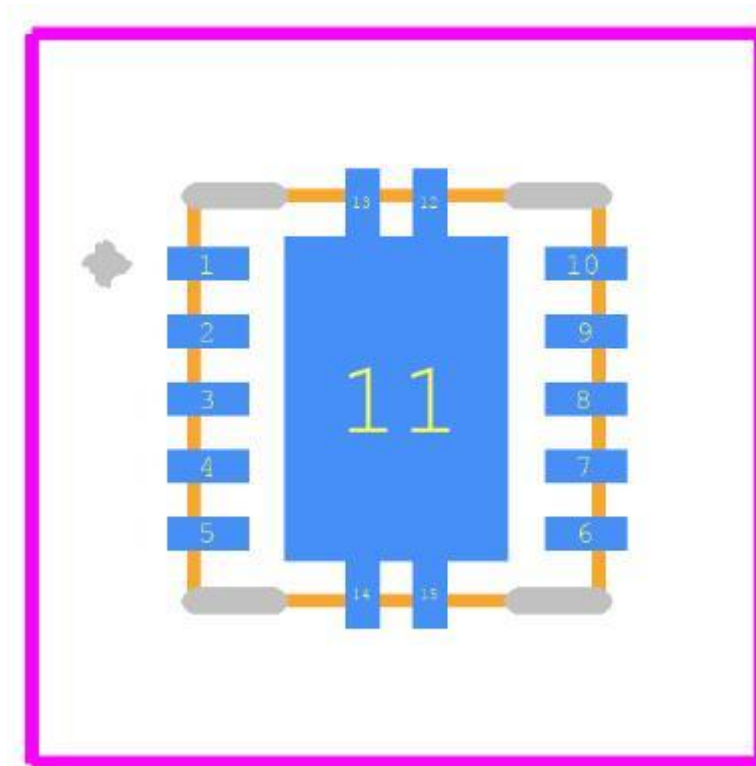
Comparison with Other Controllers

Image					
Part Number	TPS51200DRCR	LM317LBDR2G	NCP51200MNTXG	LM78L12ACMX/NOPB	NCP51400MNTXG
Manufacturer	Texas Instruments	ON Semiconductor	ON Semiconductor	Texas Instruments	ON Semiconductor
Package / Case	10-VFDFN Exposed Pad	8-SOIC (0.154, 3.90mm Width)	10-VFDFN Exposed Pad	8-SOIC (0.154, 3.90mm Width)	10-VFDFN Exposed Pad
Number of Pins	10	8	10	8	10
Number of Outputs	1	1	1	1	1
Output Current	3 A	-	3 A	-	3 A
Max Output Current	3 A	100 mA	3 A	100 mA	3 A
Min Input Voltage	2.3 V	1.3 V	2.375 V	13.7 V	2.375 V
Max Input Voltage	3.5 V	-	5.5 V	-	5.5 V
Output Voltage	3.5 V	37 V	-	12 V	1.8 V
Nominal Output Vo...	1.25 V	-	-	12 V	-
View Compare		TPS51200DRCR VS LM317LBDR2G	TPS51200DRCR VS NCP51200MNTXG	TPS51200DRCR VS LM78L12ACMX/NOPB	TPS51200DRCR VS NCP51400MNTXG

Symbol

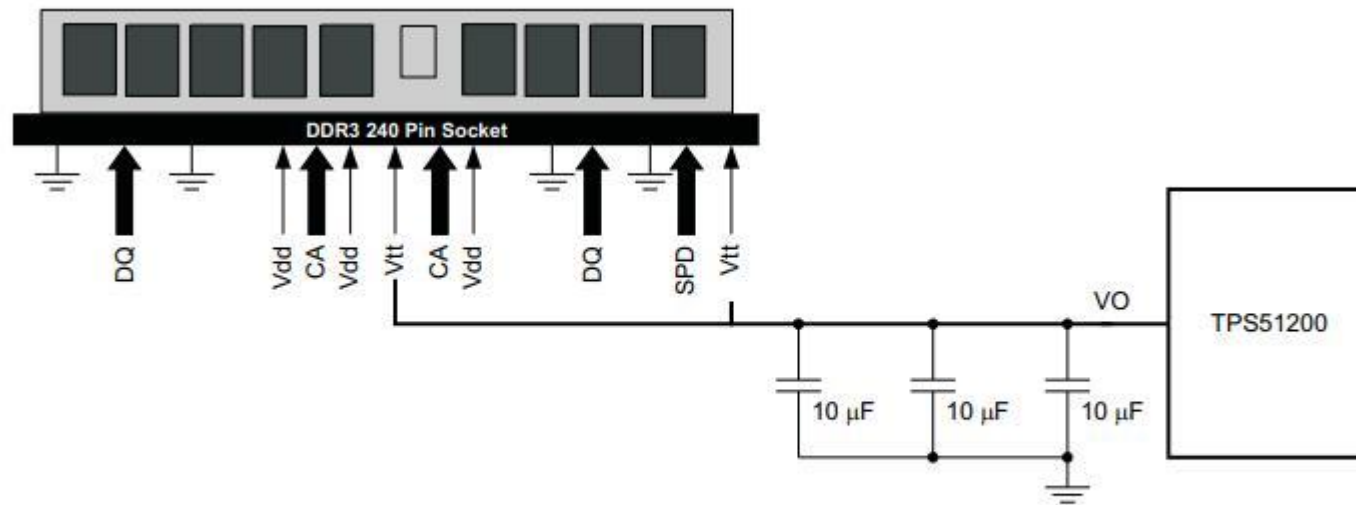


Footprint



How to Use

In figure 1, the TPS51200 device is specifically designed to power up the memory termination rail. The characteristics of the VVT rail are determined by the DDR memory termination structure. This structure is also able to sink and source current while maintaining acceptable VTT tolerance.



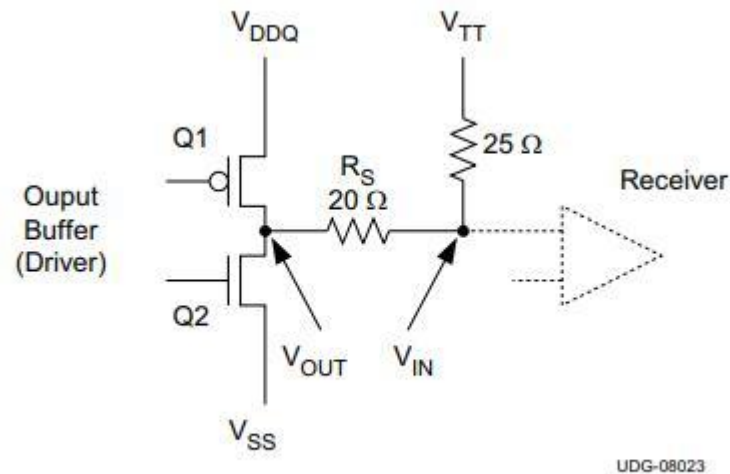
UDG-08022

Figure 1. Typical Application Diagram for DDR3 VTT DIMM using TPS51200

How to Use

Typical characteristics for a single memory cell are shown in Figure 2. When Q1 is on and Q2 is off, the current flows from VDDQ via the termination resistor to VTT, and VTT sinks the current.

When Q1 is off and Q2 is on, the current flows from VTT via the termination resistor to GND, and VTT sources the current.



UDG-08023

Figure 2. DDR Physical Signal System Bi-Directional SSTL Signaling

Layout Guidelines

The following points summarized by Easybom should be taken into consideration before starting the TPS51200 layout design.

1. Place the input bypass capacitor for VLDOIN and the output capacitor for VO as close as possible to the pin with short and wide connections.
2. If the ESR of the VO output capacitor(s) is larger than 2 mΩ, add a low-pass filter at VOSNS which be connected to the positive node of VO output capacitor(s) to avoid additional ESR and/or ESL.
3. Prepare the thermal land to dissipate heat from the package.

Conclusion

Sink/source DDR termination regulators TPS51200DRCR are designed for specific purposes depending on their special specifications and reliable performance. It is a good choice for people who need for sink/source DDR termination regulators to design their projects.