SLRS027R – DECEMBER 1976 – REVISED FEBRUARY 2024

ULN200x, ULQ200x High-Voltage, High-Current Darlington Transistor Arrays

1 Features

- 500-mA-Rated Collector Current (Single Output)
- High-Voltage Outputs: 50 V
- Output Clamp Diodes
- Inputs Compatible With Various Types of Logic
- Relay-Driver Applications

2 Applications

- Relay Drivers
- Stepper and DC Brushed Motor Drivers
- Lamp Drivers
- Display Drivers (LED and Gas Discharge)
- Line Drivers
- Logic Buffers

3 Description

The ULx200xA devices are high-voltage, high-current Darlington transistor arrays. Each consists of seven NPN Darlington pairs that feature high-voltage outputs with common-cathode clamp diodes for switching inductive loads.

The collector-current rating of a single Darlington pair is 500 mA. The Darlington pairs can be paralleled for higher current capability. Applications include relay drivers, hammer drivers, lamp drivers, display drivers (LED and gas discharge), line drivers, and logic buffers. For 100-V (otherwise interchangeable) versions of the ULx2003A devices, see the SLRS023 data sheet for the SN75468 and SN75469 devices.

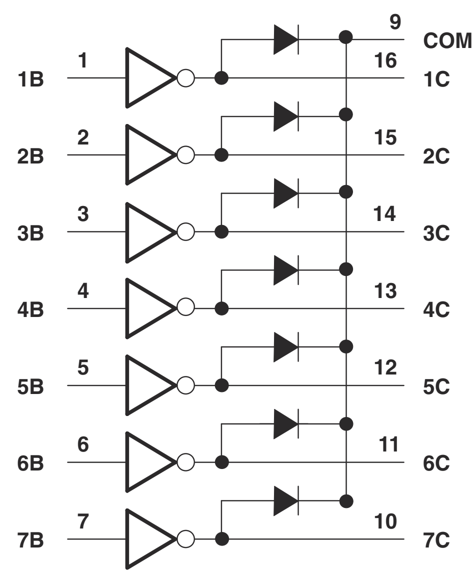
The ULN2002A device is designed specifically for use with 14-V to 25-V PMOS devices. Each input of this device has a Zener diode and resistor in series to control the input current to a safe limit. The ULx2003A devices have a 2.7-kΩ series base resistor for each Darlington pair for operation directly with TTL or 5-V CMOS devices.

The ULx2004A devices have a 10.5-kΩ series base resistor to allow operation directly from CMOS devices that use supply voltages of 6 V to 15 V. The required input current of the ULx2004A device is below that of the ULx2003A devices, and the required voltage is less than that required by the ULN2002A device.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
ULx200xD	SOIC (16)	9.90 mm × 3.91 mm
ULx200xN	PDIP (16)	19.30 mm × 6.35 mm
ULN200xNS	SOP (16)	10.30 mm × 5.30 mm
ULN200xPW	TSSOP (16)	5.00 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Block Diagram

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4 Pin Configuration and Functions

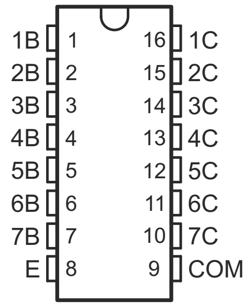


Figure 4-1. D, N, NS, and PW Package 16-Pin SOIC, PDIP, SO, and TSSOP Top View

Table 4-1. Pin Functions

PIN		I/O[1]	DESCRIPTION
NAME	NO.		
1B	1	I	Channel 1 through 7 Darlington base input
2B	2		
3B	3		
4B	4		
5B	5		
6B	6		
7B	7		
1C	16	O	Channel 1 through 7 Darlington collector output
2C	15		
3C	14		
4C	13		
5C	12		
6C	11		
7C	10		
COM	9	—	Common cathode node for flyback diodes (required for inductive loads)
E	8	—	Common emitter shared by all channels (typically tied to ground)

(1) I = Input, O = Output

5 Specifications

5.1 Absolute Maximum Ratings

at 25°C free-air temperature (unless otherwise noted)[(1)]

			MIN	MAX	UNIT
V_{CC}	Collector-emitter voltage			50	V
	Clamp diode reverse voltage[(2)]			50	V
V_I	Input voltage[(2)]			30	V
	Peak collector current, See Figure 5-4 and Figure 5-5			500	mA
I_{OK}	Output clamp current			500	mA
	Total emitter-terminal current			–2.5	A
T_A	Operating free-air temperature range	ULN200xA	–40	70	°C
		ULN200xAI	–40	105	
		ULQ200xA	–40	85	
		ULQ200xAT	–40	105	
T_J	Operating virtual junction temperature			150	°C
	Lead temperature for 1.6 mm (1/16 inch) from case for 10 seconds			260	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the emitter/substrate terminal E, unless otherwise noted.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[(1)]	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101[(2)]	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Collector-emitter voltage (non-V devices)	0	50	V
T_J	Junction temperature	–40	125	°C

5.4 Thermal Information

THERMAL METRIC[(1)]		ULx200x				UNIT
		D (SOIC)	N (PDIP)	NS (SO)	PW (TSSOP)	
		16 PINS	16 PINS	16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	88.6	66.7	95	114.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	50.1	54.2	53.3	50.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	49.8	46.7	57.2	59.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	12.4	33.7	19.6	9.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	49.3	46.4	56.8	58.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

5.5 Electrical Characteristics: ULN2002A

T_A = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS		ULN2002A MIN	ULN2002A TYP	ULN2002A MAX	UNIT
$V_{I(on)}$	ON-state input voltage	Figure 6-6	V_{CE} = 2 V,	I_C = 300 mA			13	V
V_{OH}	High-level output voltage after switching	Figure 6-10	V_S = 50 V, I_O = 300 mA		V_S – 20			mV
$V_{CE(sat)}$	Collector-emitter saturation voltage	Figure 6-4	I_I = 250 µA,	I_C = 100 mA		0.9	1.1	V
			I_I = 350 µA,	I_C = 200 mA		1	1.3	
			I_I = 500 µA,	I_C = 350 mA		1.2	1.6	
V_F	Clamp forward voltage	Figure 6-7	I_F = 350 mA			1.7	2	V
I_{CEX}	Collector cutoff current	Figure 6-1	V_{CE} = 50 V,	I_I = 0			50	µA
		Figure 6-2	V_{CE} = 50 V, T_A = 70°C	I_I = 0			100	
				V_I = 6 V			500	
$I_{I(off)}$	OFF-state input current	Figure 6-2	V_{CE} = 50 V,	I_C = 500 µA	50	65		µA
I_I	Input current	Figure 6-3	V_I = 17 V			0.82	1.25	mA
I_R	Clamp reverse current	Figure 6-6	V_R = 50 V	T_A = 70°C			100	µA
			V_R = 50 V				50	
C_i	Input capacitance		V_I = 0,	f = 1 MHz			25	pF

5.6 Electrical Characteristics: ULN2003A and ULN2004A

T_A = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS		ULN2003A MIN	ULN2003A TYP	ULN2003A MAX	ULN2004A MIN	ULN2004A TYP	ULN2004A MAX	UNIT
$V_{I(on)}$	ON-state input voltage	Figure 6-6	V_{CE} = 2 V	I_C = 125 mA						5	V
				I_C = 200 mA			2.4			6	
				I_C = 250 mA			2.7				
				I_C = 275 mA						7	
				I_C = 300 mA			3				
				I_C = 350 mA						8	
V_{OH}	High-level output voltage after switching	Figure 6-10	V_S = 50 V, I_O = 300 mA		V_S – 20			V_S – 20			mV
$V_{CE(sat)}$	Collector-emitter saturation voltage	Figure 6-5	I_I = 250 µA,	I_C = 100 mA		0.9	1.1		0.9	1.1	V
			I_I = 350 µA,	I_C = 200 mA		1	1.3		1	1.3	
			I_I = 500 µA,	I_C = 350 mA		1.2	1.6		1.2	1.6	
I_{CEX}	Collector cutoff current	Figure 6-1	V_{CE} = 50 V,	I_I = 0			50			50	µA
		Figure 6-2	V_{CE} = 50 V, T_A = 70°C	I_I = 0			100			100	
				V_I = 6 V						500	
V_F	Clamp forward voltage	Figure 6-8	I_F = 350 mA			1.7	2		1.7	2	V
$I_{I(off)}$	Off-state input current	Figure 6-3	V_{CE} = 50 V, T_A = 70°C,	I_C = 500 µA	50	65		50	65		µA
I_I	Input current	Figure 6-4	V_I = 3.85 V			0.93	1.35				mA
			V_I = 5 V						0.35	0.5	
			V_I = 12 V						1	1.45	
I_R	Clamp reverse current	Figure 6-7	V_R = 50 V				50			50	µA
			V_R = 50 V	T_A = 70°C			100			100	

5.6 Electrical Characteristics: ULN2003A and ULN2004A (continued)

T_A = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS		ULN2003A			ULN2004A			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
C_i	Input capacitance		V_I = 0,	f = 1 MHz		15	25		15	25	pF

5.7 Electrical Characteristics: ULN2003AI

T_A = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS		ULN2003AI			UNIT
					MIN	TYP	MAX	
$V_{I(on)}$	ON-state input voltage	Figure 6-6	V_{CE} = 2 V	I_C = 200 mA			2.4	V
				I_C = 250 mA			2.7	
				I_C = 300 mA			3	
V_{OH}	High-level output voltage after switching	Figure 6-10	V_S = 50 V, I_O = 300 mA		V_S – 50			mV
$V_{CE(sat)}$	Collector-emitter saturation voltage	Figure 6-5	I_I = 250 µA,	I_C = 100 mA		0.9	1.1	V
			I_I = 350 µA,	I_C = 200 mA		1	1.3	
			I_I = 500 µA,	I_C = 350 mA		1.2	1.6	
I_{CEX}	Collector cutoff current	Figure 6-1	V_{CE} = 50 V,	I_I = 0			50	µA
V_F	Clamp forward voltage	Figure 6-8	I_F = 350 mA			1.7	2	V
$I_{I(off)}$	OFF-state input current	Figure 6-3	V_{CE} = 50 V,	I_C = 500 µA	50	65		µA
I_I	Input current	Figure 6-4	V_I = 3.85 V			0.93	1.35	mA
I_R	Clamp reverse current	Figure 6-7	V_R = 50 V				50	µA
C_i	Input capacitance		V_I = 0,	f = 1 MHz		15	25	pF

5.8 Electrical Characteristics: ULN2003AI

T_A = –40°C to 105°C

PARAMETER		TEST FIGURE	TEST CONDITIONS		ULN2003AI			UNIT
					MIN	TYP	MAX	
$V_{I(on)}$	ON-state input voltage	Figure 6-6	V_{CE} = 2 V	I_C = 200 mA			2.7	V
				I_C = 250 mA			2.9	
				I_C = 300 mA			3	
V_{OH}	High-level output voltage after switching	Figure 6-10	V_S = 50 V, I_O = 300 mA		V_S – 50			mV
$V_{CE(sat)}$	Collector-emitter saturation voltage	Figure 6-5	I_I = 250 µA,	I_C = 100 mA		0.9	1.2	V
			I_I = 350 µA,	I_C = 200 mA		1	1.4	
			I_I = 500 µA,	I_C = 350 mA		1.2	1.7	
I_{CEX}	Collector cutoff current	Figure 6-1	V_{CE} = 50 V,	I_I = 0			100	µA
V_F	Clamp forward voltage	Figure 6-8	I_F = 350 mA			1.7	2.2	V
$I_{I(off)}$	OFF-state input current	Figure 6-3	V_{CE} = 50 V,	I_C = 500 µA	30	65		µA
I_I	Input current	Figure 6-4	V_I = 3.85 V			0.93	1.35	mA
I_R	Clamp reverse current	Figure 6-7	V_R = 50 V				100	µA
C_i	Input capacitance		V_I = 0,	f = 1 MHz		15	25	pF

5.9 Electrical Characteristics: ULQ2003A and ULQ2004A

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS		ULQ2003A MIN	ULQ2003A TYP	ULQ2003A MAX	ULQ2004A MIN	ULQ2004A TYP	ULQ2004A MAX	UNIT
$V_{I(on)}$	ON-state input voltage	Figure 6-6	V_{CE} = 2 V	I_C = 125 mA						5	V
				I_C = 200 mA			2.7			6	
				I_C = 250 mA			2.9				
				I_C = 275 mA						7	
				I_C = 300 mA			3				
				I_C = 350 mA						8	
V_{OH}	High-level output voltage after switching	Figure 6-10	V_S = 50 V, I_O = 300 mA		V_S – 50			V_S – 50			mV
$V_{CE(sat)}$	Collector-emitter saturation voltage	Figure 6-5	I_I = 250 µA,	I_C = 100 mA		0.9	1.2		0.9	1.1	V
			I_I = 350 µA,	I_C = 200 mA		1	1.4		1	1.3	
			I_I = 500 µA,	I_C = 350 mA		1.2	1.7		1.2	1.6	
I_{CEX}	Collector cutoff current	Figure 6-1	V_{CE} = 50 V,	I_I = 0			100			50	µA
		Figure 6-2	V_{CE} = 50 V, T_A = 70°C	I_I = 0						100	
				V_I = 6 V						500	
V_F	Clamp forward voltage	Figure 6-8	I_F = 350 mA			1.7	2.3		1.7	2	V
$I_{I(off)}$	OFF-state input current	Figure 6-3	V_{CE} = 50 V, T_A = 70°C,	I_C = 500 µA		65		50	65		µA
I_I	Input current	Figure 6-4	V_I = 3.85 V			0.93	1.35				mA
			V_I = 5 V						0.35	0.5	
			V_I = 12 V						1	1.45	
I_R	Clamp reverse current	Figure 6-7	V_R = 50 V	T_A = 25°C			100			50	µA
			V_R = 50 V				100			100	
C_i	Input capacitance		V_I = 0,	f = 1 MHz		15	25		15	25	pF

5.10 Switching Characteristics: ULN2002A, ULN2003A, ULN2004A

T_A = 25°C

PARAMETER		TEST CONDITIONS	ULN2002A, ULN2003A, ULN2004A MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	See Figure 6-9		0.25	1	µs
t_{PHL}	Propagation delay time, high- to low-level output	See Figure 6-9		0.25	1	µs

5.11 Switching Characteristics: ULN2003AI

T_A = 25°C

PARAMETER		TEST CONDITIONS	ULN2003AI MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	See Figure 6-9		0.25	1	µs
t_{PHL}	Propagation delay time, high- to low-level output	See Figure 6-9		0.25	1	µs

5.12 Switching Characteristics: ULN2003AI

T_A = –40°C to 105°C

PARAMETER		TEST CONDITIONS	ULN2003AI			UNIT
			MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low- to high-level output	See Figure 6-9		1	10	μs
t_{PHL}	Propagation delay time, high- to low-level output	See Figure 6-9		1	10	μs

5.13 Switching Characteristics: ULQ2003A, ULQ2004A

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	ULQ2003A, ULQ2004A			UNIT
			MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low- to high-level output	See Figure 6-9		1	10	μs
t_{PHL}	Propagation delay time, high- to low-level output	See Figure 6-9		1	10	μs

5.14 Typical Characteristics

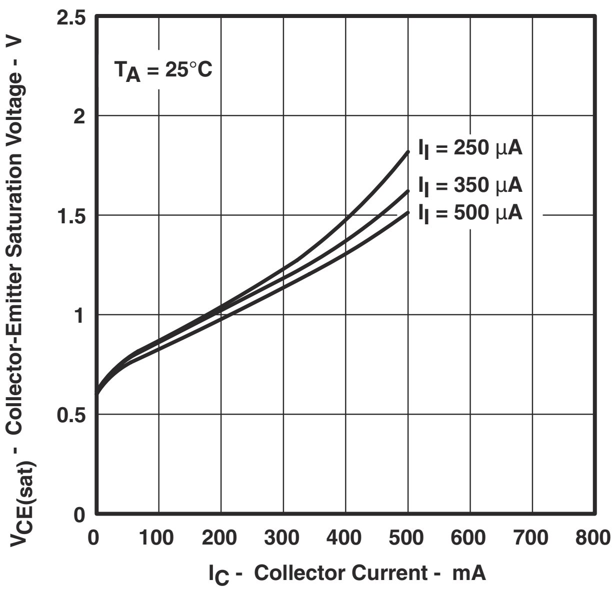


Figure 5-1. Collector-Emitter Saturation Voltage vs Collector Current (One Darlington)

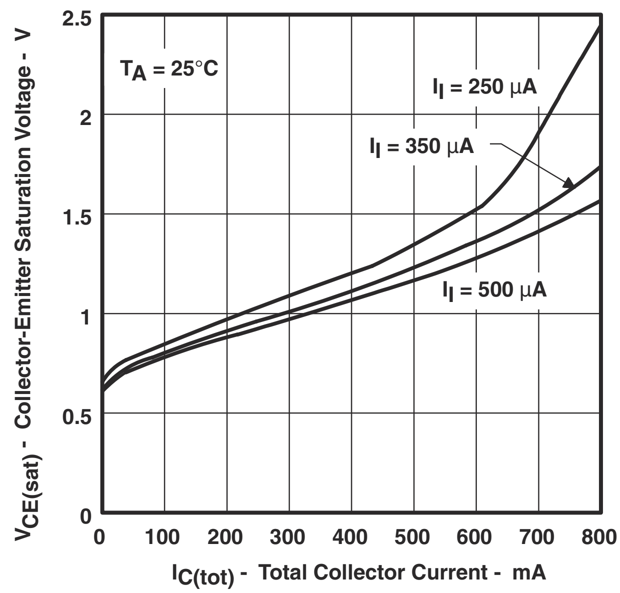


Figure 5-2. Collector-Emitter Saturation Voltage vs Total Collector Current (Two Darlingtons in Parallel)

5.14 Typical Characteristics (continued)

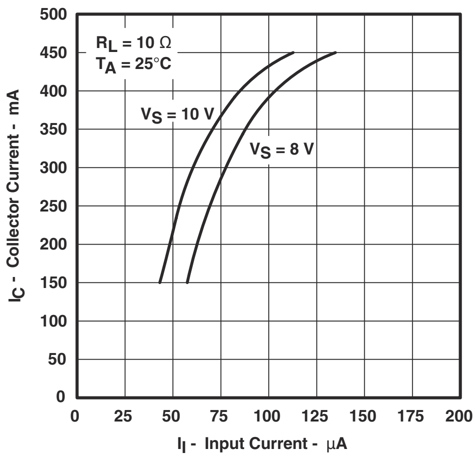


Figure 5-3. Collector Current vs Input Current

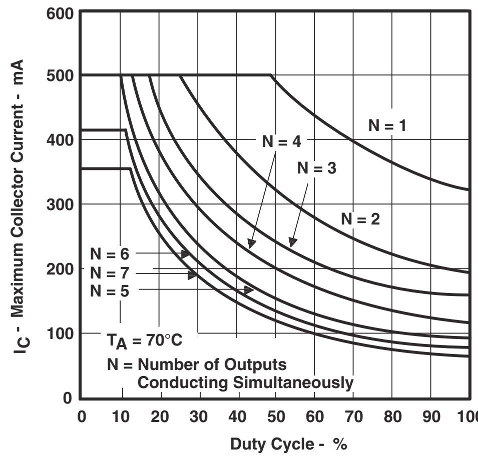


Figure 5-4. D Package Maximum Collector Current vs Duty Cycle

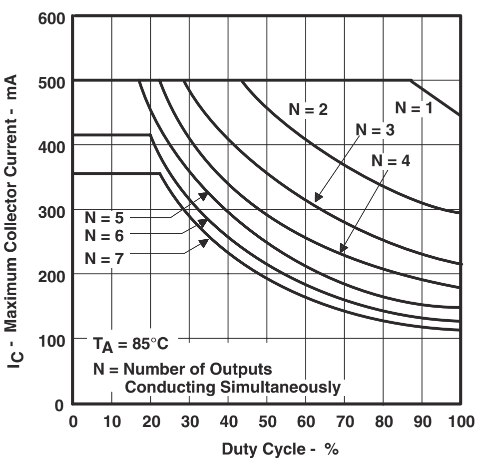


Figure 5-5. N Package Maximum Collector Current vs Duty Cycle

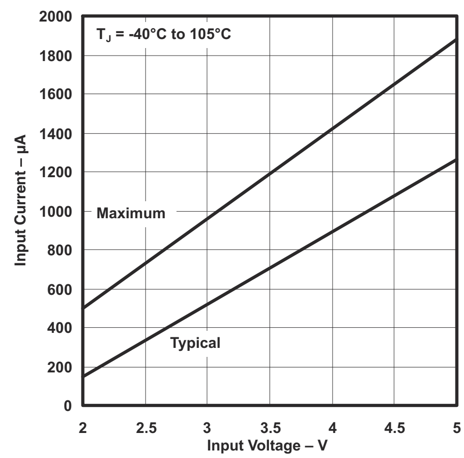


Figure 5-6. Maximum and Typical Input Current vs Input Voltage

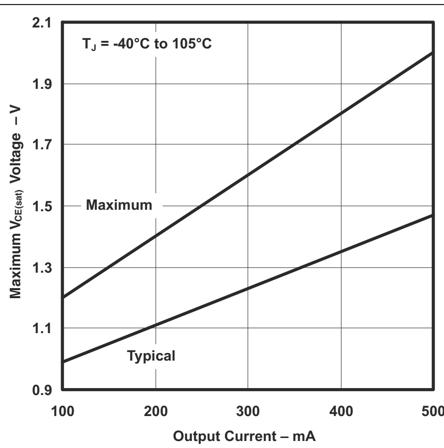


Figure 5-7. Maximum and Typical Saturated V_{CE} vs Output Current

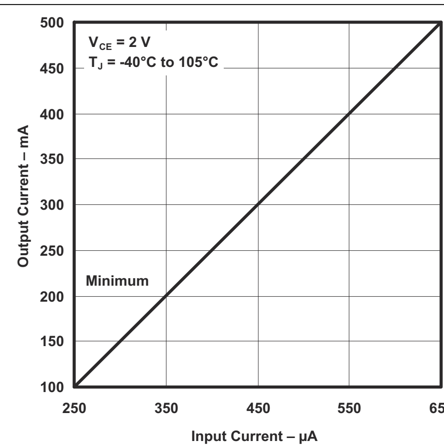


Figure 5-8. Minimum Output Current vs Input Current

6 Parameter Measurement Information

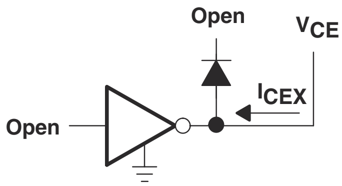


Figure 6-1. I_{CEX} Test Circuit

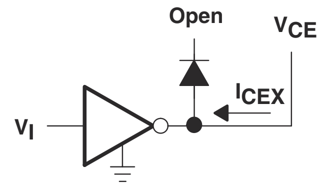


Figure 6-2. I_{CEX} Test Circuit

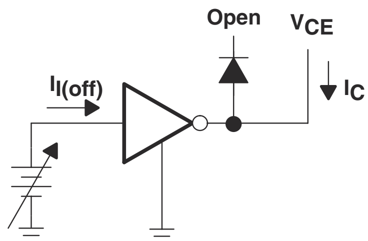


Figure 6-3. $I_{I(off)}$ Test Circuit

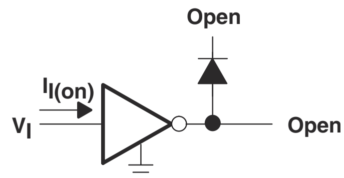
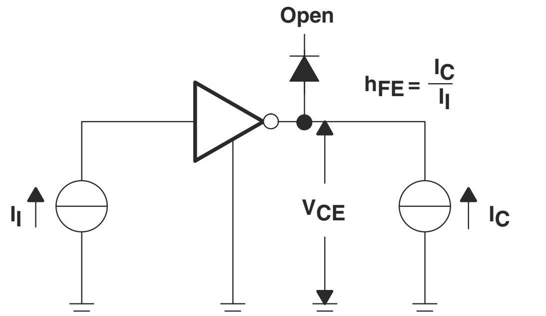


Figure 6-4. I_I Test Circuit



I_I is fixed for measuring $V_{CE(sat)}$, variable for measuring h_{FE}.

Figure 6-5. h_{FE}, $V_{CE(sat)}$ Test Circuit

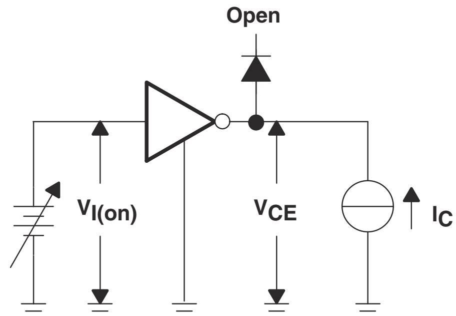


Figure 6-6. $V_{I(on)}$ Test Circuit

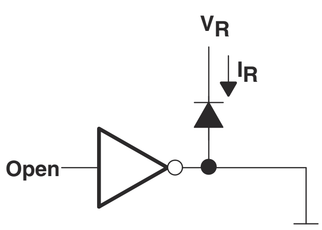


Figure 6-7. I_R Test Circuit

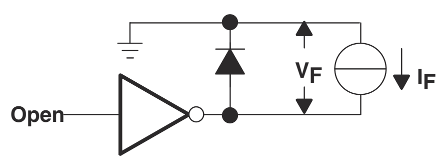


Figure 6-8. V_F Test Circuit

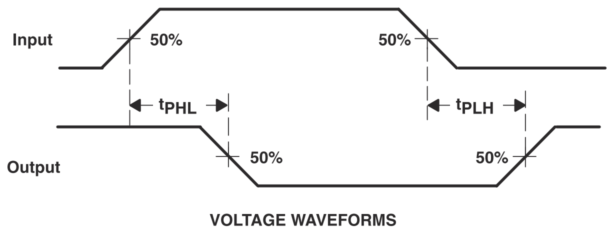
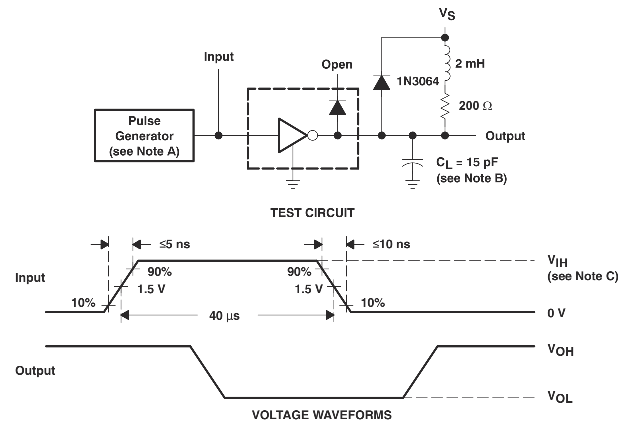


Figure 6-9. Propagation Delay-Time Waveforms



The pulse generator has the following characteristics: PRR = 12.5 kHz, Z_O = 50 Ω.

C_L includes probe and jig capacitance.

For testing the ULN2003A device, ULN2003AI device, and ULQ2003A devices, V_{IH} = 3 V; for the ULN2002A device, V_{IH} = 13 V; for the ULN2004A and the ULQ2004A devices, V_{IH} = 8 V.

Figure 6-10. Latch-Up Test Circuit and Voltage Waveforms

7 Detailed Description

7.1 Overview

This standard device has proven ubiquity and versatility across a wide range of applications. This is due to integration of 7 Darlington transistors of the device that are capable of sinking up to 500 mA and wide GPIO range capability.

The ULN2003A device comprises seven high-voltage, high-current NPN Darlington transistor pairs. All units feature a common emitter and open collector outputs. To maximize their effectiveness, these units contain suppression diodes for inductive loads. The ULN2003A device has a series base resistor to each Darlington pair, thus allowing operation directly with TTL or CMOS operating at supply voltages of 5 V or 3.3 V. The ULN2003A device offers solutions to a great many interface needs, including solenoids, relays, lamps, small motors, and LEDs. Applications requiring sink currents beyond the capability of a single output may be accommodated by paralleling the outputs.

This device can operate over a wide temperature range (–40°C to 105°C).

7.2 Functional Block Diagrams

All resistor values shown are nominal. The collector-emitter diode is a parasitic structure and should not be used to conduct current. If the collectors go below GND, an external Schottky diode should be added to clamp negative undershoots.

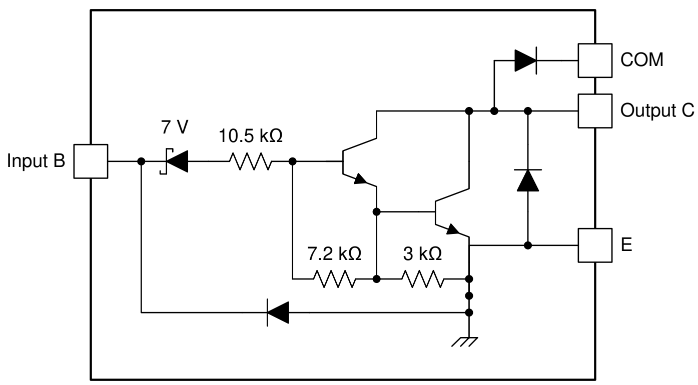


Figure 7-1. ULN2002A Block Diagram

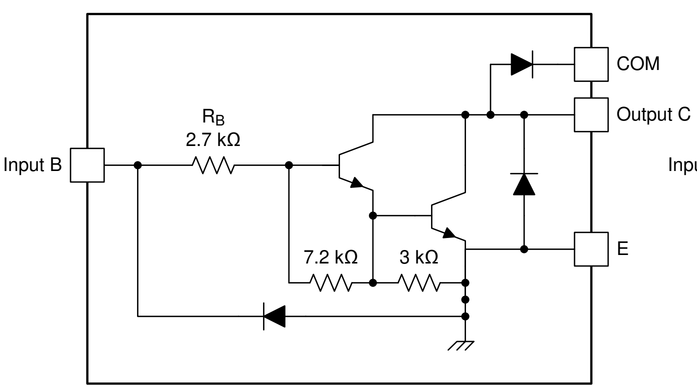


Figure 7-2. ULN2003A, ULQ2003A and ULN2003AI Block Diagram

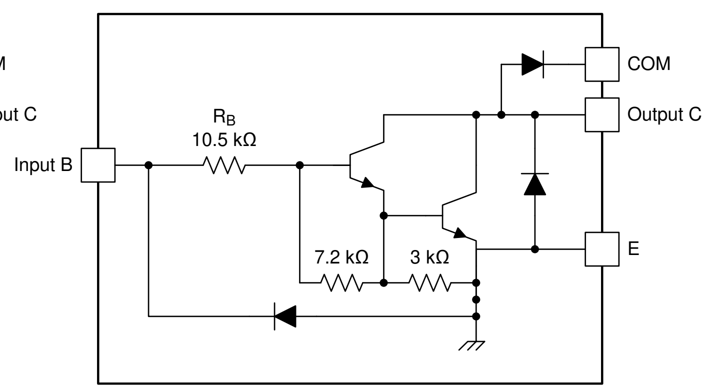


Figure 7-3. ULN2004A and LQ2004A Block Diagram

7.3 Feature Description

Each channel of the ULN2003A device consists of Darlington connected NPN transistors. This connection creates the effect of a single transistor with a very high-current gain (β2). This can be as high as 10,000 A/A at certain currents. The very high β allows for high-output current drive with a very low input current, essentially equating to operation with low GPIO voltages.

The GPIO voltage is converted to base current through the 2.7-kΩ resistor connected between the input and base of the predriver Darlington NPN. The 7.2-kΩ and 3-kΩ resistors connected between the base and emitter of each respective NPN act as pulldowns and suppress the amount of leakage that may occur from the input.

The diodes connected between the output and COM pin is used to suppress the kick-back voltage from an inductive load that is excited when the NPN drivers are turned off (stop sinking) and the stored energy in the coils causes a reverse current to flow into the coil supply through the kick-back diode.

In normal operation the diodes on base and collector pins to emitter will be reversed biased. If these diodes are forward biased, internal parasitic NPN transistors will draw (a nearly equal) current from other (nearby) device pins.

7.4 Device Functional Modes

7.4.1 Inductive Load Drive

When the COM pin is tied to the coil supply voltage, ULN2003A device is able to drive inductive loads and suppress the kick-back voltage through the internal free-wheeling diodes.

7.4.2 Resistive Load Drive

When driving a resistive load, a pullup resistor is needed in order for ULN2003A device to sink current and for there to be a logic high level. The COM pin can be left floating for these applications.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

Typically, the ULN2003A device drives a high-voltage or high-current (or both) peripheral from an MCU or logic device that cannot tolerate these conditions. This design is a common application of ULN2003A device, driving inductive loads. This includes motors, solenoids and relays. Figure 8-1 shows a model for each load type.

8.2 Typical Application

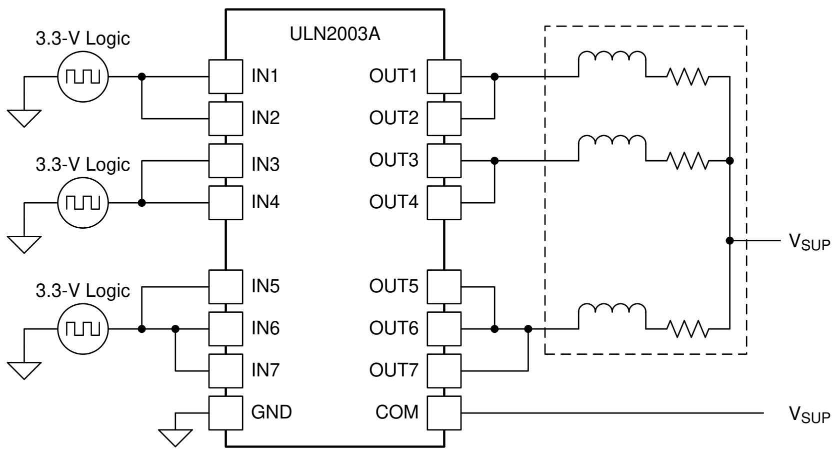


Figure 8-1. ULN2003A Device as Inductive Load Driver

8.2.1 Design Requirements

For this design example, use the parameters listed in Table 8-1 as the input parameters.

Table 8-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
GPIO voltage	3.3 V or 5 V
Coil supply voltage	12 V to 48 V
Number of channels	7
Output current (R_{COIL})	20 mA to 300 mA per channel
Duty cycle	100%

8.2.2 Detailed Design Procedure

When using ULN2003A device in a coil driving application, determine the following:

- Input voltage range
- Temperature range
- Output and drive current
- Power dissipation

8.2.2.1 Drive Current

The coil voltage (V_{SUP}), coil resistance (R_{COIL}), and low-level output voltage ($V_{CE(SAT)}$ or V_{OL}) determine the coil current.

$$I_{COIL} = (V_{SUP} - V_{CE(SAT)}) / R_{COIL} \tag{1}$$

8.2.2.2 Low-Level Output Voltage

The low-level output voltage (V_{OL}) is the same as $V_{CE(SAT)}$ and can be determined by, Figure 5-1, Figure 5-2, or Figure 5-7.

8.2.2.3 Power Dissipation and Temperature

The number of coils driven is dependent on the coil current and on-chip power dissipation. The number of coils driven can be determined by Figure 5-4 or Figure 5-5.

For a more accurate determination of number of coils possible, use the below equation to calculate ULN2003A device on-chip power dissipation P_D:

$$P_D = \sum_{i=1}^{N} V_{OLi} \times I_{Li} \tag{2}$$

where

- N is the number of channels active together
- V_{OLi} is the OUT_i pin voltage for the load current I_{Li}. This is the same as $V_{CE(SAT)}$

To ensure reliability of ULN2003A device and the system, the on-chip power dissipation must be lower that or equal to the maximum allowable power dissipation ($PD_{(MAX)}$) dictated by below equation Equation 3.

$$PD_{(MAX)} = \frac{\left(T_{J(MAX)} - T_A\right)}{\theta_{JA}} \tag{3}$$

where

- $T_{J(max)}$ is the target maximum junction temperature
- T_A is the operating ambient temperature
- $R_{\theta JA}$ is the package junction to ambient thermal resistance

Limit the die junction temperature of the ULN2003A device to less than 125°C. The IC junction temperature is directly proportional to the on-chip power dissipation.

8.2.3 Application Curves

The characterization data shown in Figure 8-2 and Figure 8-3 were generated using the ULN2003A device driving an OMRON G5NB relay and under the following conditions: V_{IN} = 5 V, V_{SUP}= 12 V, and R_{COIL}= 2.8 kΩ.

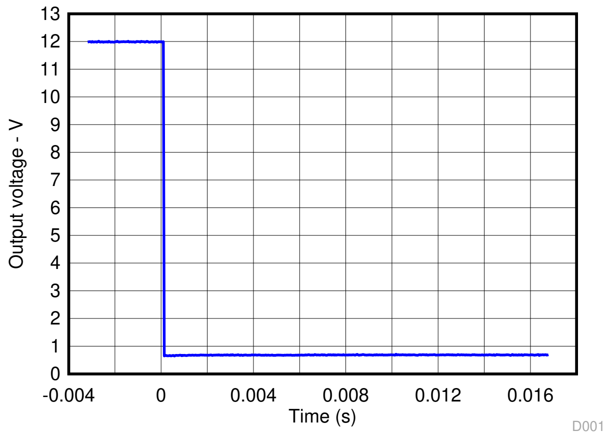


Figure 8-2. Output Response With Activation of Coil (Turnon)

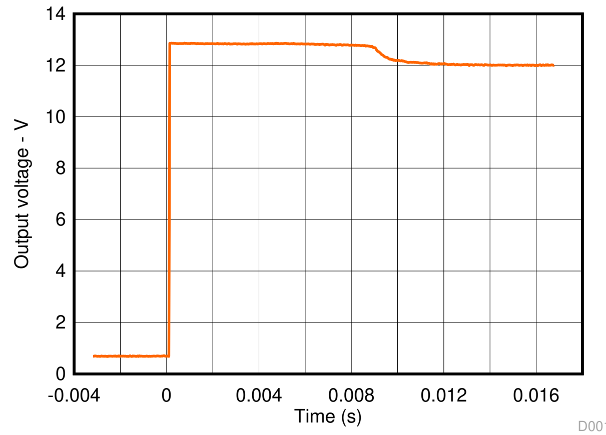


Figure 8-3. Output Response With De-activation of Coil (Turnoff)

8.3 System Examples

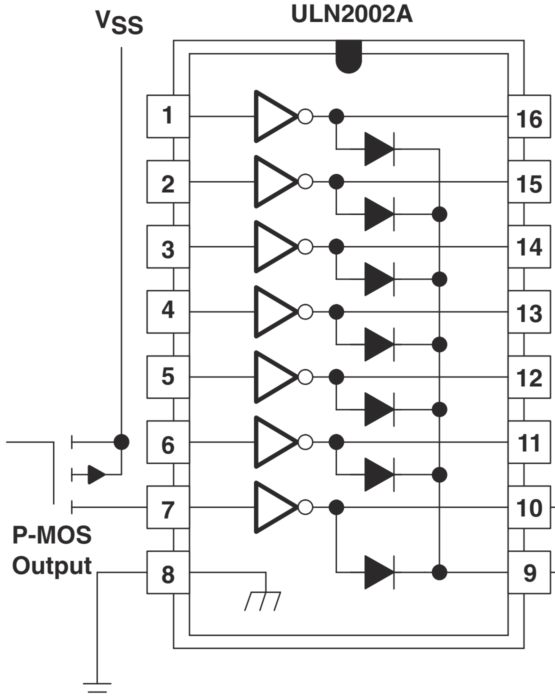


Figure 8-4. P-MOS to Load

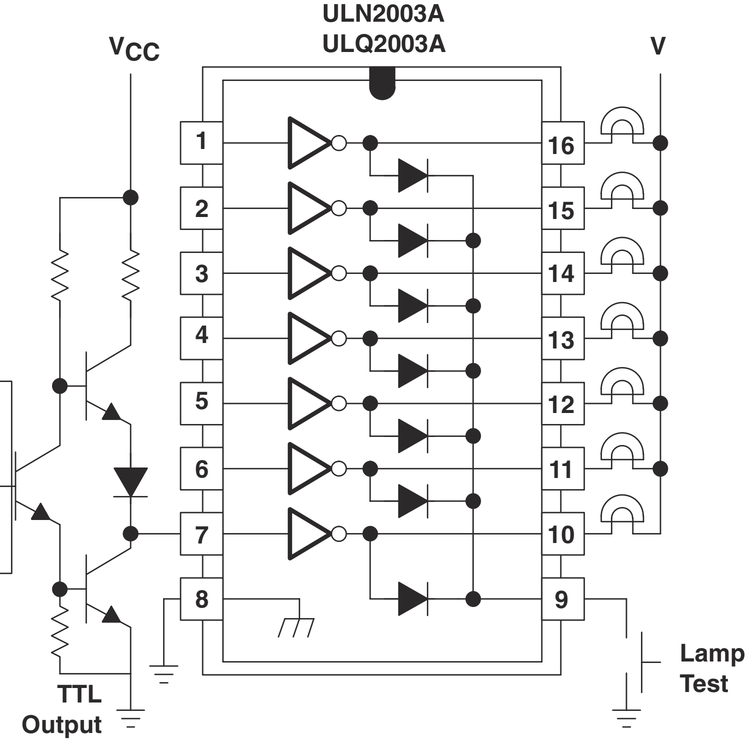


Figure 8-5. TTL to Load

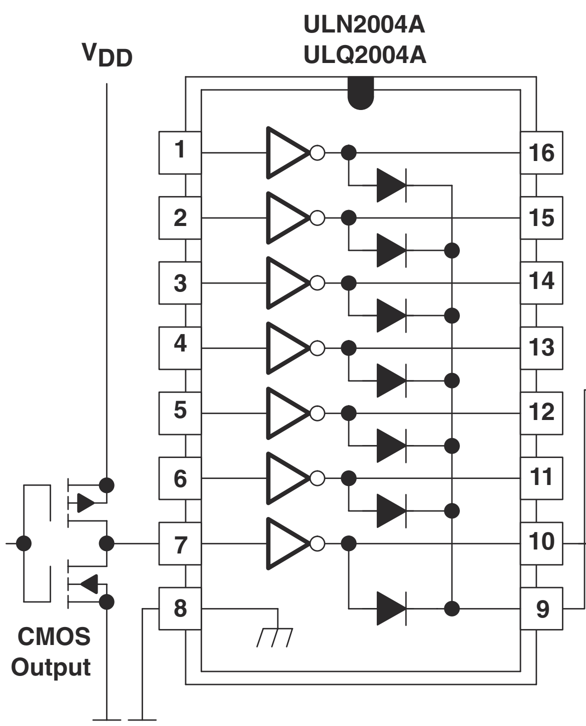


Figure 8-6. Buffer for Higher Current Loads

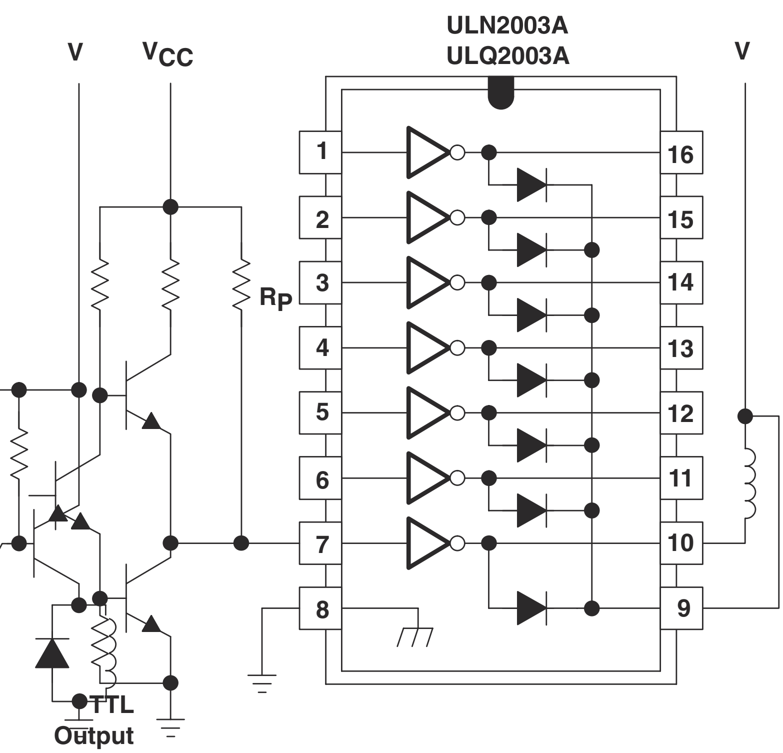


Figure 8-7. Use of Pullup Resistors to Increase Drive Current

9 Power Supply Recommendations

This device does not need a power supply. However, the COM pin is typically tied to the system power supply. When this is the case, it is very important to ensure that the output voltage does not heavily exceed the COM pin voltage. This discrepancy heavily forward biases the fly-back diodes and causes a large current to flow into COM, potentially damaging the on-chip metal or over-heating the device.

10 Layout

10.1 Layout Guidelines

Thin traces can be used on the input due to the low-current logic that is typically used to drive ULN2003A device. Take care to separate the input channels as much as possible, as to eliminate crosstalk. TI recommends thick traces for the output to drive whatever high currents that may be needed. Wire thickness can be determined by the current density of the trace material and desired drive current.

Because all of the channels currents return to a common emitter, it is best to size that trace width to be very wide. Some applications require up to 2.5 A.

10.2 Layout Example

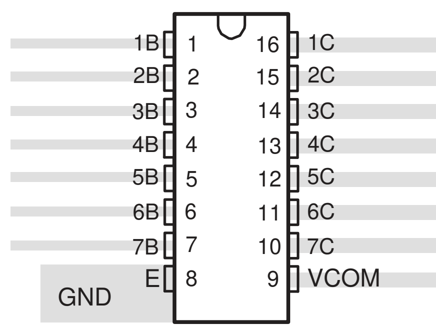


Figure 10-1. Package Layout

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation, see the following:

SN7546x Darlington Transistor Arrays, SLRS023

11.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 11-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
ULN2002A	Click here	Click here	Click here	Click here	Click here
ULN2003A	Click here	Click here	Click here	Click here	Click here
ULN2003AI	Click here	Click here	Click here	Click here	Click here
ULN2004A	Click here	Click here	Click here	Click here	Click here
ULQ2003A	Click here	Click here	Click here	Click here	Click here
ULQ2004A	Click here	Click here	Click here	Click here	Click here

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

11.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

12 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ULN2002AN	LIFEBUY	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-20 to 70	ULN2002AN	
ULN2002ANE4	LIFEBUY	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-20 to 70	ULN2002AN	
ULN2003AD	LIFEBUY	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 70	ULN2003A	
ULN2003ADE4	LIFEBUY	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 70	ULN2003A	
ULN2003ADR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 70	ULN2003A	Samples
ULN2003ADRE4	LIFEBUY	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 70	ULN2003A	
ULN2003ADRG3	LIFEBUY	SOIC	D	16	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 70	ULN2003A	
ULN2003ADRG4	LIFEBUY	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 70	ULN2003A	
ULN2003AID	LIFEBUY	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	ULN2003AI	
ULN2003AIDE4	LIFEBUY	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	ULN2003AI	
ULN2003AIDG4	LIFEBUY	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	ULN2003AI	
ULN2003AIDR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 105	ULN2003AI	Samples
ULN2003AIDRE4	LIFEBUY	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	ULN2003AI	
ULN2003AIDRG4	LIFEBUY	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	ULN2003AI	
ULN2003AIN	LIFEBUY	PDIP	N	16	25	RoHS & Green	NIPDAU | SN	N / A for Pkg Type	-40 to 105	ULN2003AIN	
ULN2003AINE4	LIFEBUY	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 105	ULN2003AIN	
ULN2003AINSR	ACTIVE	SO	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	ULN2003AI	Samples
ULN2003AIPW	LIFEBUY	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	UN2003AI	
ULN2003AIPWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 105	UN2003AI	Samples
ULN2003AIPWRG4	LIFEBUY	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	UN2003AI	
ULN2003AN	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU | SN	N / A for Pkg Type	-40 to 70	ULN2003AN	Samples
ULN2003ANE4	LIFEBUY	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 70	ULN2003AN	
ULN2003ANS	LIFEBUY	SO	NS	16	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 70	ULN2003A	
ULN2003ANSR	ACTIVE	SO	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 70	ULN2003A	Samples
ULN2003ANSRE4	ACTIVE	SO	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 70	ULN2003A	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ULN2003ANSRG4	ACTIVE	SO	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 70	ULN2003A	Samples
ULN2003APW	LIFEBUY	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 70	UN2003A	
ULN2003APWG4	LIFEBUY	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 70	UN2003A	
ULN2003APWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 70	UN2003A	Samples
ULN2003APWRG4	LIFEBUY	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 70	UN2003A	
ULN2004AD	LIFEBUY	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-20 to 70	ULN2004A	
ULN2004ADE4	LIFEBUY	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-20 to 70	ULN2004A	
ULN2004ADG4	LIFEBUY	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-20 to 70	ULN2004A	
ULN2004ADR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-20 to 70	ULN2004A	Samples
ULN2004ADRE4	LIFEBUY	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-20 to 70	ULN2004A	
ULN2004ADRG4	LIFEBUY	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-20 to 70	ULN2004A	
ULN2004AN	LIFEBUY	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-20 to 70	ULN2004AN	
ULN2004ANE4	LIFEBUY	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-20 to 70	ULN2004AN	
ULN2004ANS	LIFEBUY	SO	NS	16	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		ULN2004A	
ULN2004ANSR	LIFEBUY	SO	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-20 to 70	ULN2004A	
ULQ2003AD	LIFEBUY	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ULQ2003A	
ULQ2003ADG4	LIFEBUY	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		ULQ2003A	
ULQ2003ADR	LIFEBUY	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ULQ2003A	
ULQ2003ADRG4	LIFEBUY	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		ULQ2003A	
ULQ2003AN	LIFEBUY	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	ULQ2003A	
ULQ2004AD	LIFEBUY	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ULQ2004A	
ULQ2004ADR	LIFEBUY	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ULQ2004A	
ULQ2004ADRG4	LIFEBUY	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		ULQ2004A	
ULQ2004AN	LIFEBUY	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	ULQ2004AN	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF ULQ2003A, ULQ2004A :

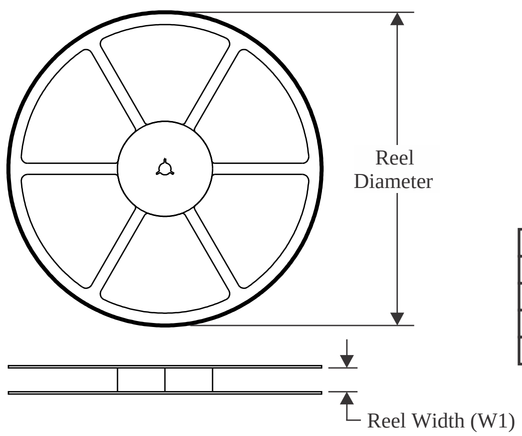
- Automotive : ULQ2003A-Q1, ULQ2004A-Q1

NOTE: Qualified Version Definitions:

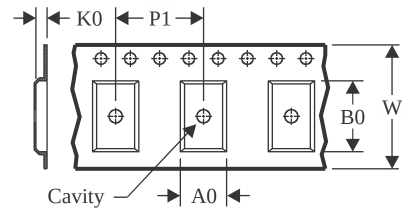
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

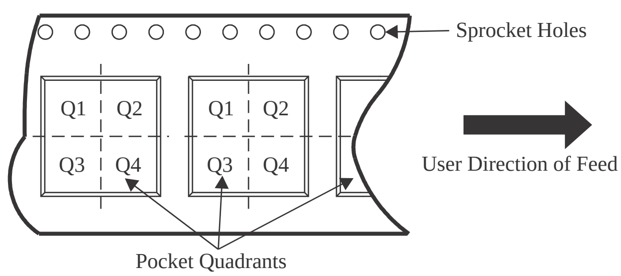


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

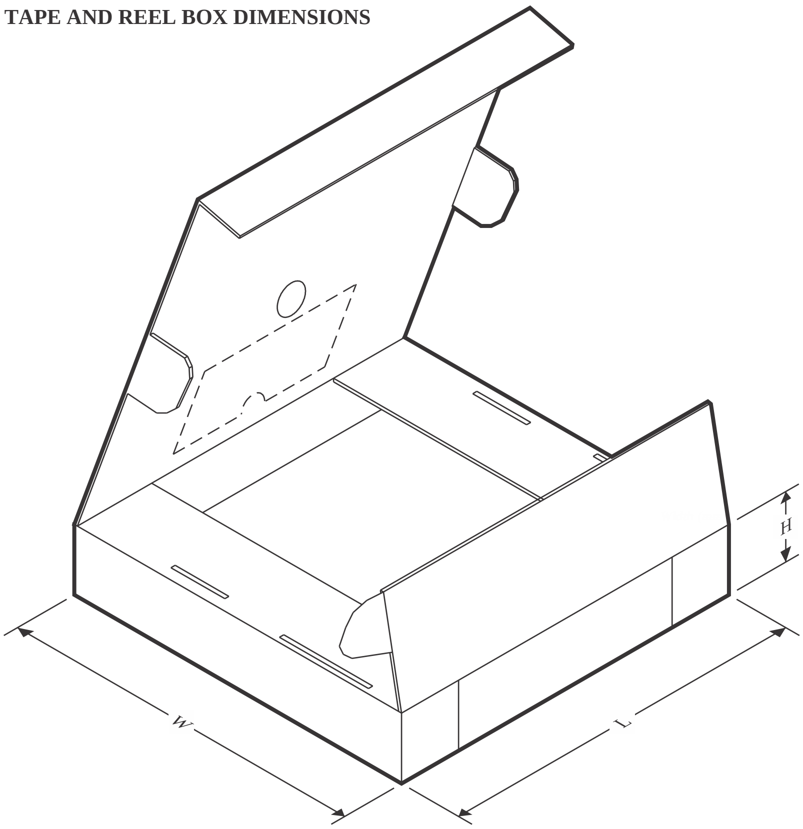


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ULN2003ADR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
ULN2003ADR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
ULN2003ADRG3	SOIC	D	16	2500	330.0	16.8	6.5	10.3	2.1	8.0	16.0	Q1
ULN2003ADRG4	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
ULN2003ADRG4	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
ULN2003AIDR	SOIC	D	16	2500	330.0	16.8	6.5	10.3	2.1	8.0	16.0	Q1
ULN2003AIDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
ULN2003AIDRG4	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
ULN2003AINSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
ULN2003AIPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
ULN2003AIPWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
ULN2003ANSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
ULN2003APWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
ULN2003APWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
ULN2004ADR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
ULN2004ADR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ULN2004ADRG4	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
ULN2004ADRG4	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
ULN2004ANSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
ULQ2003ADR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
ULQ2003ADRG4	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

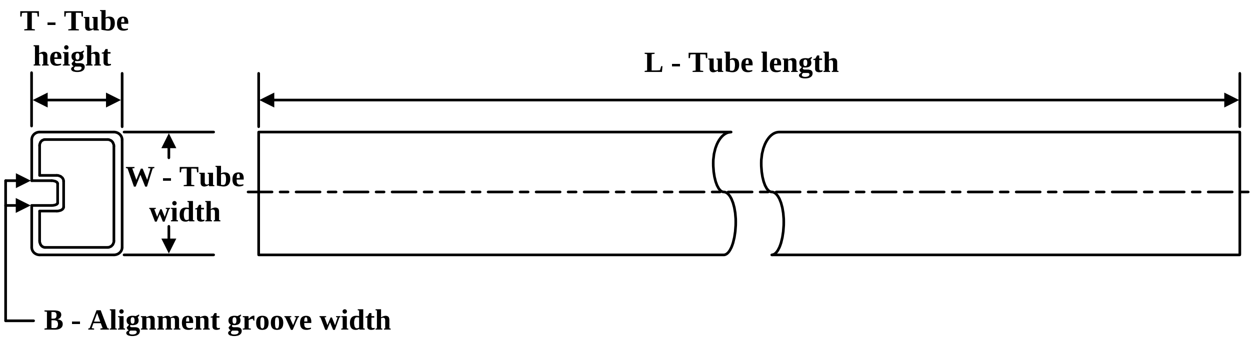


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ULN2003ADR	SOIC	D	16	2500	356.0	356.0	35.0
ULN2003ADR	SOIC	D	16	2500	340.5	336.1	32.0
ULN2003ADRG3	SOIC	D	16	2500	364.0	364.0	27.0
ULN2003ADRG4	SOIC	D	16	2500	340.5	336.1	32.0
ULN2003ADRG4	SOIC	D	16	2500	367.0	367.0	38.0
ULN2003AIDR	SOIC	D	16	2500	364.0	364.0	27.0
ULN2003AIDR	SOIC	D	16	2500	340.5	336.1	32.0
ULN2003AIDRG4	SOIC	D	16	2500	340.5	336.1	32.0
ULN2003AINSR	SO	NS	16	2000	356.0	356.0	35.0
ULN2003AIPWR	TSSOP	PW	16	2000	356.0	356.0	35.0
ULN2003AIPWRG4	TSSOP	PW	16	2000	356.0	356.0	35.0
ULN2003ANSR	SO	NS	16	2000	356.0	356.0	35.0
ULN2003APWR	TSSOP	PW	16	2000	356.0	356.0	35.0
ULN2003APWRG4	TSSOP	PW	16	2000	356.0	356.0	35.0
ULN2004ADR	SOIC	D	16	2500	340.5	336.1	32.0
ULN2004ADR	SOIC	D	16	2500	356.0	356.0	35.0
ULN2004ADRG4	SOIC	D	16	2500	356.0	356.0	35.0
ULN2004ADRG4	SOIC	D	16	2500	340.5	336.1	32.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ULN2004ANSR	SO	NS	16	2000	356.0	356.0	35.0
ULQ2003ADR	SOIC	D	16	2500	340.5	336.1	32.0
ULQ2003ADRG4	SOIC	D	16	2500	356.0	356.0	35.0

TUBE



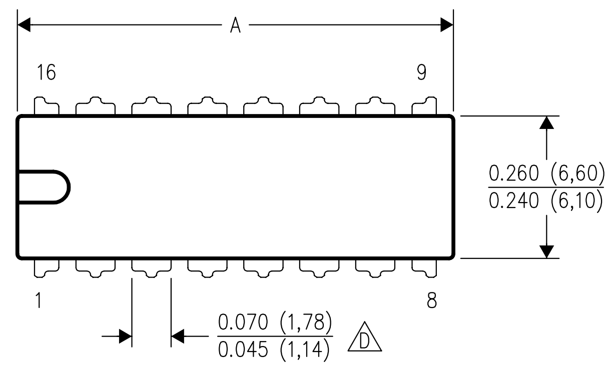
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
ULN2002AN	N	PDIP	16	25	506	13.97	11230	4.32
ULN2002ANE4	N	PDIP	16	25	506	13.97	11230	4.32
ULN2003AD	D	SOIC	16	40	507	8	3940	4.32
ULN2003AD	D	SOIC	16	40	506.6	8	3940	4.32
ULN2003ADE4	D	SOIC	16	40	507	8	3940	4.32
ULN2003ADE4	D	SOIC	16	40	506.6	8	3940	4.32
ULN2003AID	D	SOIC	16	40	507	8	3940	4.32
ULN2003AIDE4	D	SOIC	16	40	507	8	3940	4.32
ULN2003AIDG4	D	SOIC	16	40	507	8	3940	4.32
ULN2003AIN	N	PDIP	16	25	506	13.97	11230	4.32
ULN2003AIN	N	PDIP	16	25	506.1	9	600	5.4
ULN2003AIN	N	PDIP	16	25	506	13.97	11230	4.32
ULN2003AINE4	N	PDIP	16	25	506	13.97	11230	4.32
ULN2003AINE4	N	PDIP	16	25	506	13.97	11230	4.32
ULN2003AINE4	N	PDIP	16	25	506.1	9	600	5.4
ULN2003AIPW	PW	TSSOP	16	90	530	10.2	3600	3.5
ULN2003AN	N	PDIP	16	25	506	13.97	11230	4.32
ULN2003AN	N	PDIP	16	25	506	13.97	11230	4.32
ULN2003AN	N	PDIP	16	25	506.1	9	600	5.4
ULN2003ANE4	N	PDIP	16	25	506	13.97	11230	4.32
ULN2003ANS	NS	SOP	16	50	530	10.5	4000	4.1
ULN2003APW	PW	TSSOP	16	90	530	10.2	3600	3.5
ULN2003APWG4	PW	TSSOP	16	90	530	10.2	3600	3.5
ULN2004AD	D	SOIC	16	40	507	8	3940	4.32
ULN2004AD	D	SOIC	16	40	506.6	8	3940	4.32
ULN2004ADE4	D	SOIC	16	40	507	8	3940	4.32
ULN2004ADE4	D	SOIC	16	40	506.6	8	3940	4.32
ULN2004ADG4	D	SOIC	16	40	506.6	8	3940	4.32
ULN2004ADG4	D	SOIC	16	40	507	8	3940	4.32

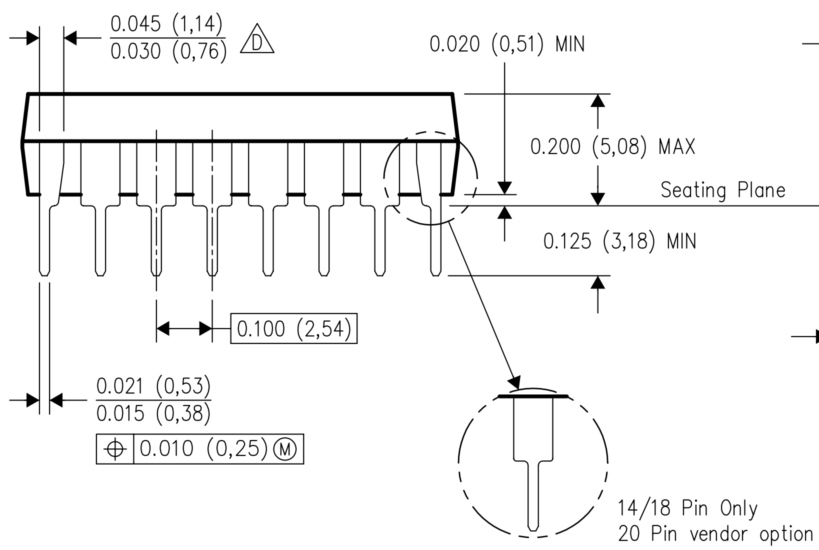
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
ULN2004AN	N	PDIP	16	25	506	13.97	11230	4.32
ULN2004AN	N	PDIP	16	25	506	13.97	11230	4.32
ULN2004ANE4	N	PDIP	16	25	506	13.97	11230	4.32
ULN2004ANE4	N	PDIP	16	25	506	13.97	11230	4.32
ULN2004ANS	NS	SOP	16	50	530	10.5	4000	4.1
ULQ2003AD	D	SOIC	16	40	507	8	3940	4.32
ULQ2003AD	D	SOIC	16	40	506.6	8	3940	4.32
ULQ2003ADG4	D	SOIC	16	40	507	8	3940	4.32
ULQ2003ADG4	D	SOIC	16	40	506.6	8	3940	4.32
ULQ2003AN	N	PDIP	16	25	506	13.97	11230	4.32
ULQ2003AN	N	PDIP	16	25	506	13.97	11230	4.32
ULQ2004AD	D	SOIC	16	40	507	8	3940	4.32
ULQ2004AN	N	PDIP	16	25	506	13.97	11230	4.32

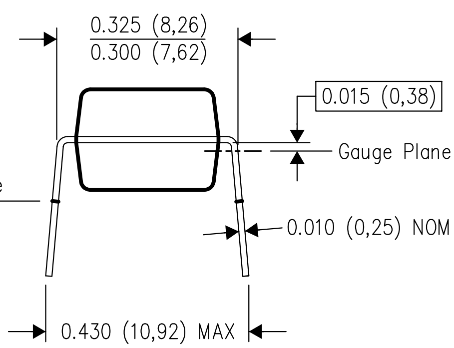
N (R–PDIP–T**) PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



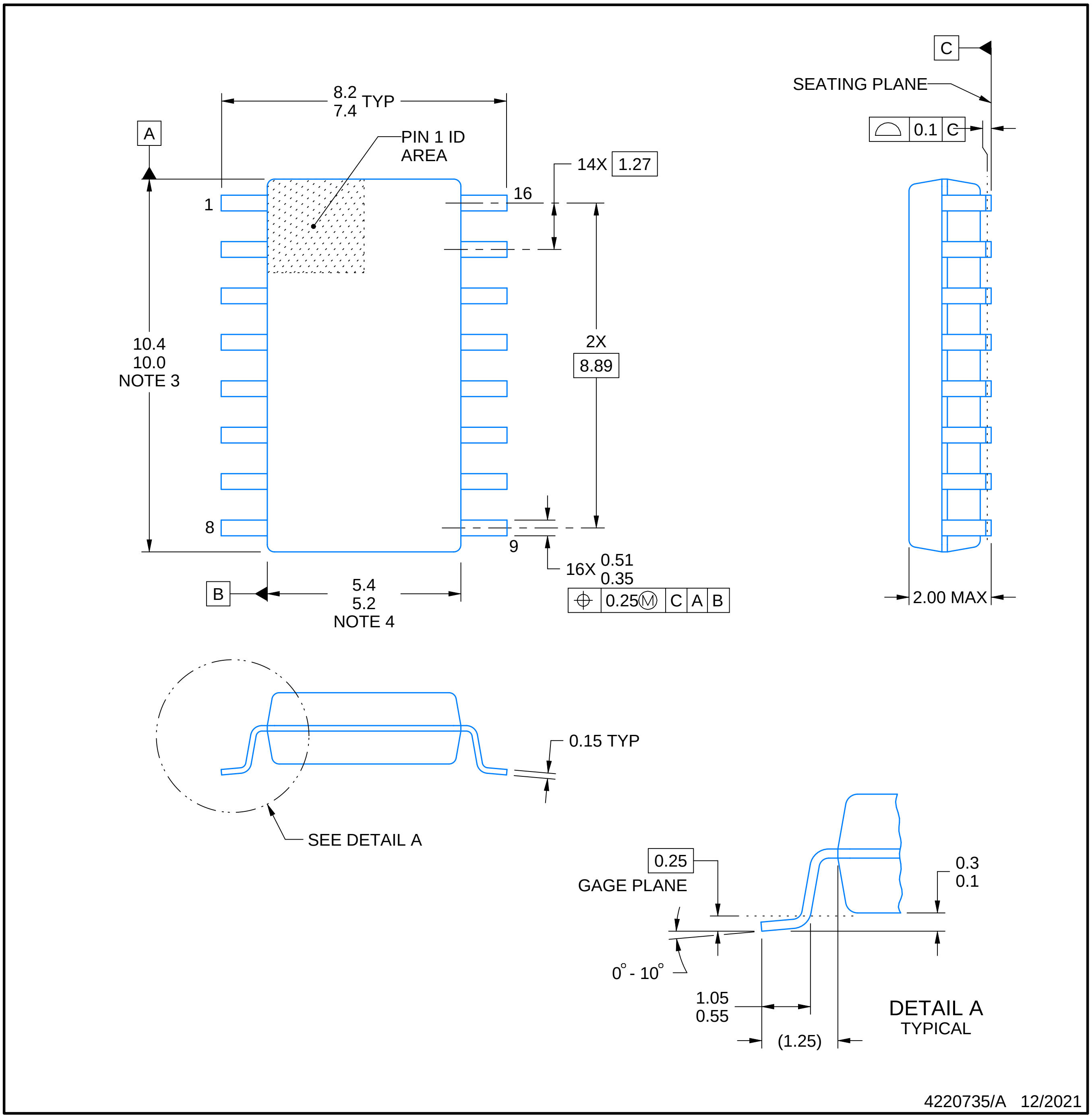
PINS ** / DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
C MS–001 VARIATION	AA	BB	AC	AD





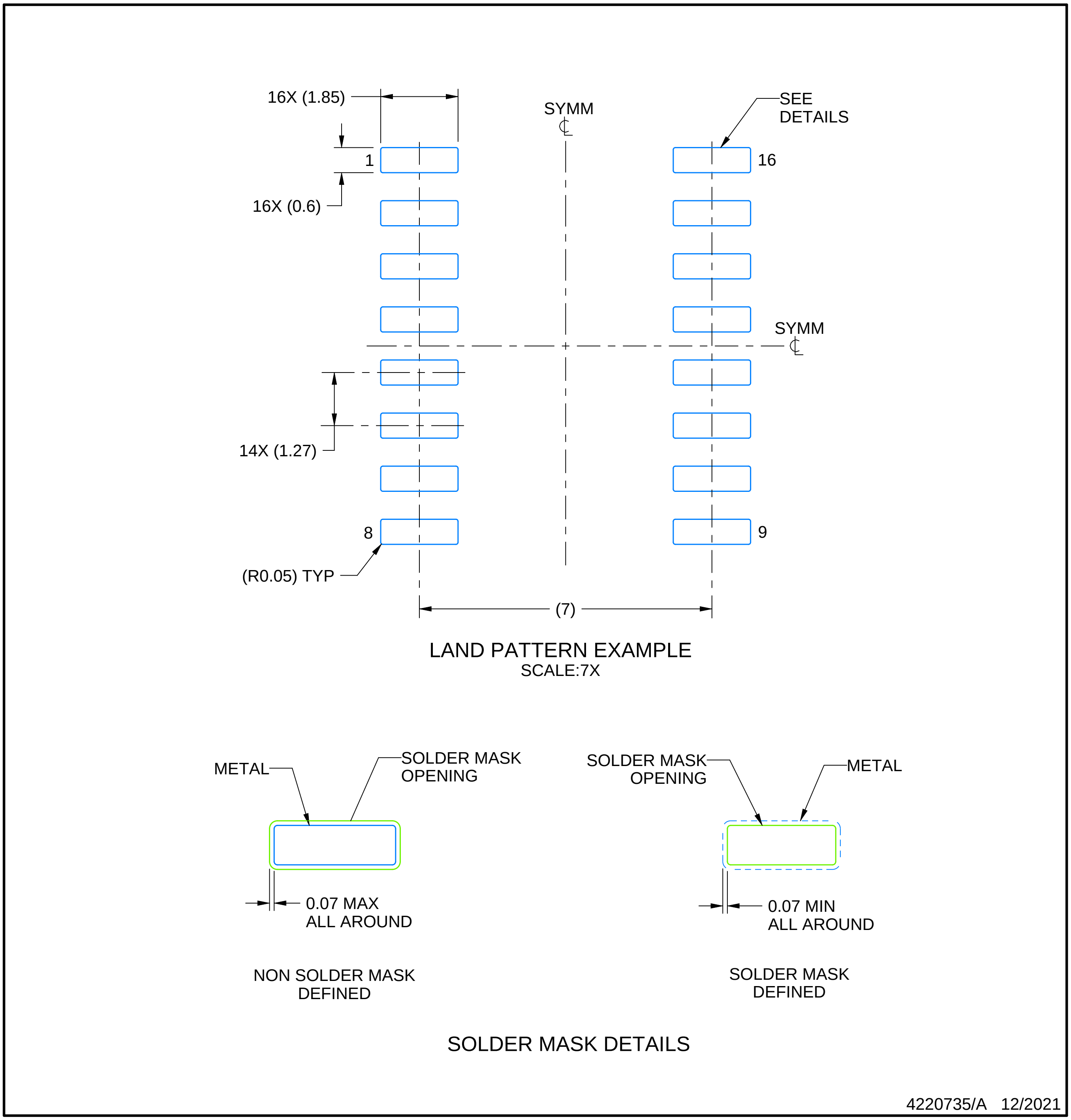
4040049/E 12/2002

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.



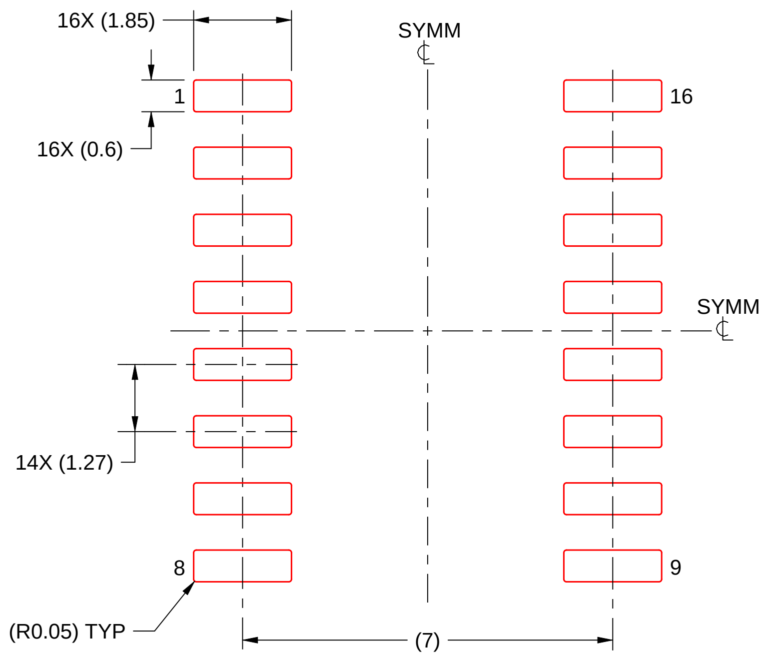
NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



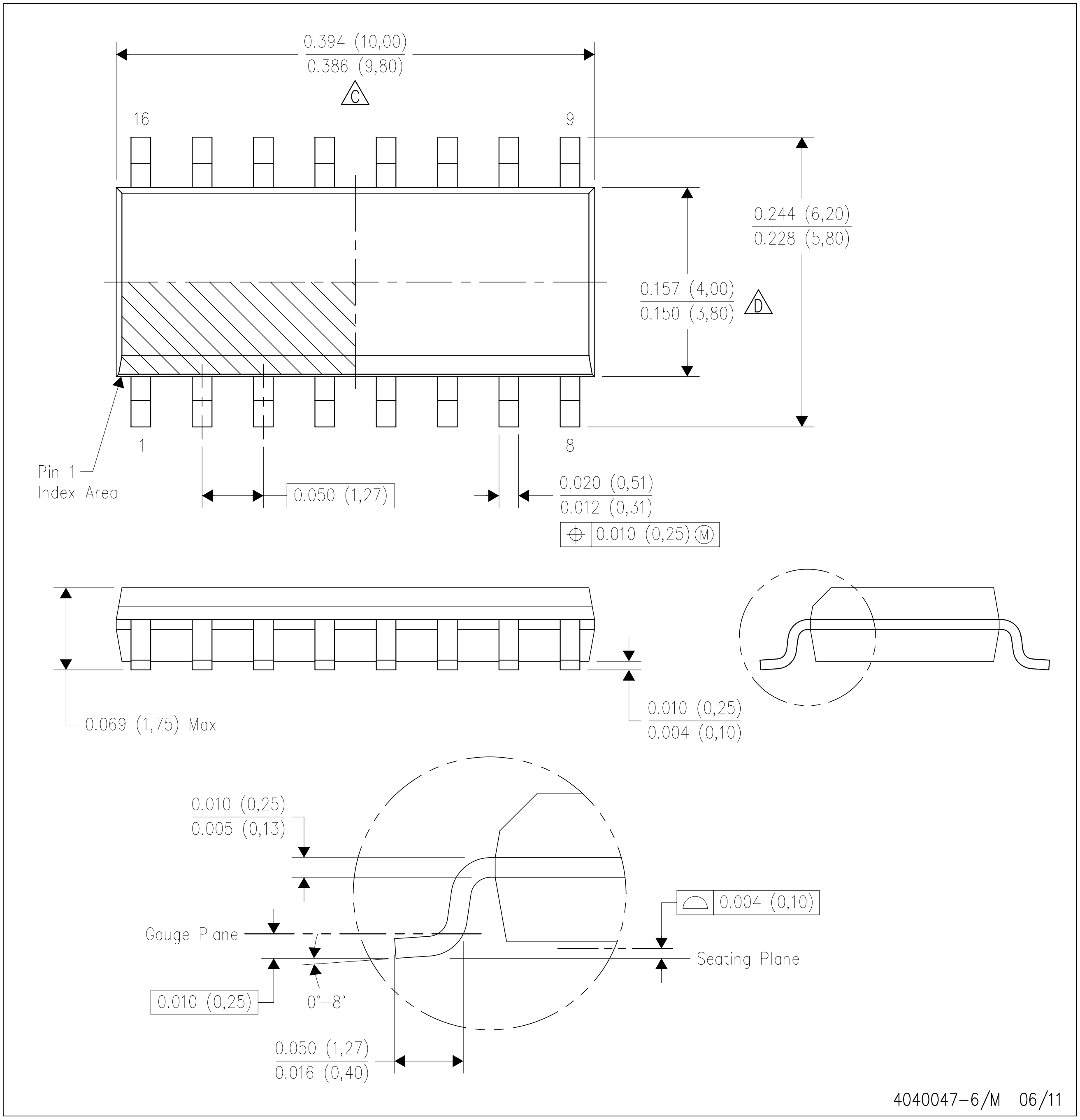
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220735/A 12/2021

NOTES: (continued)

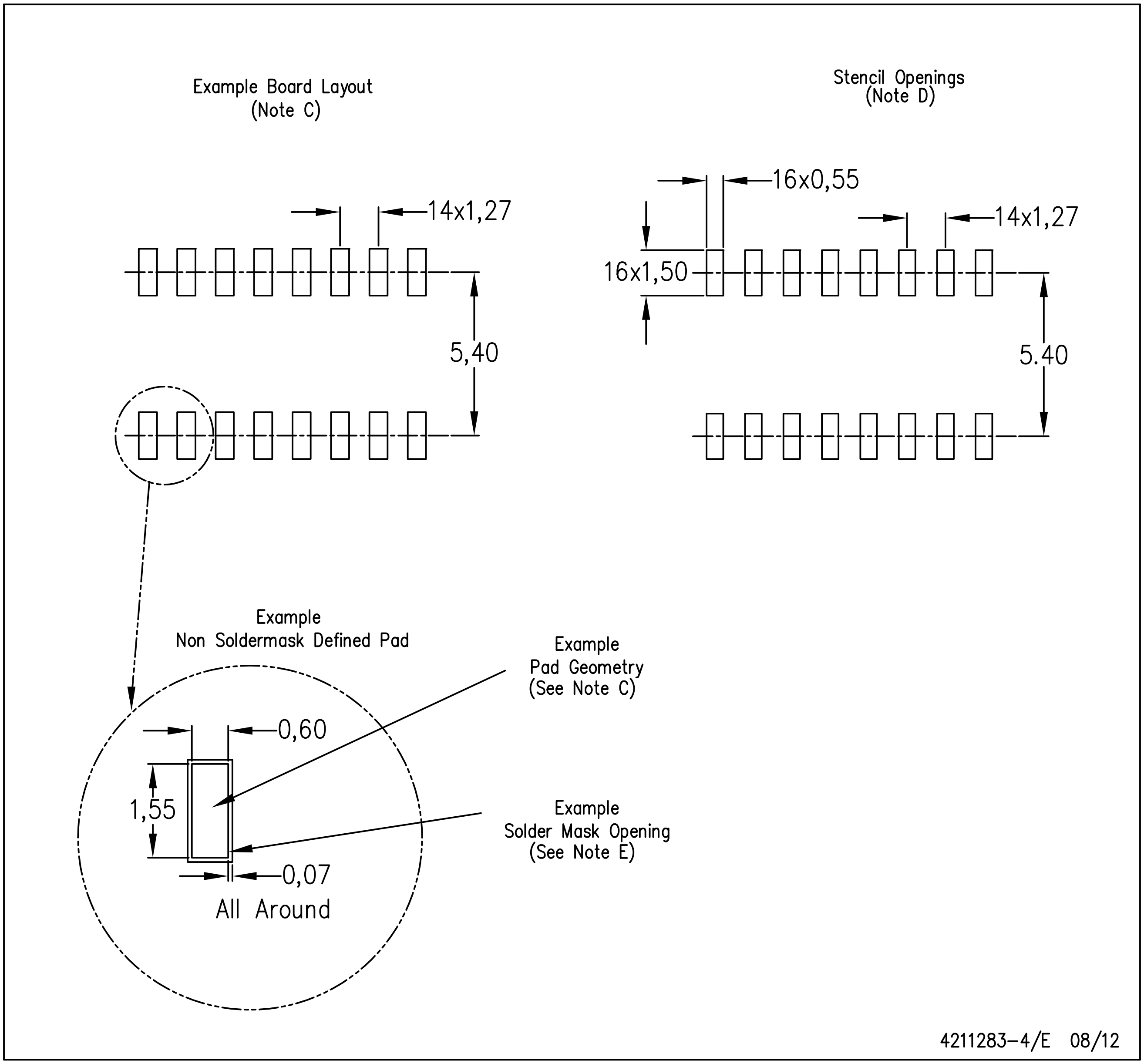
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE

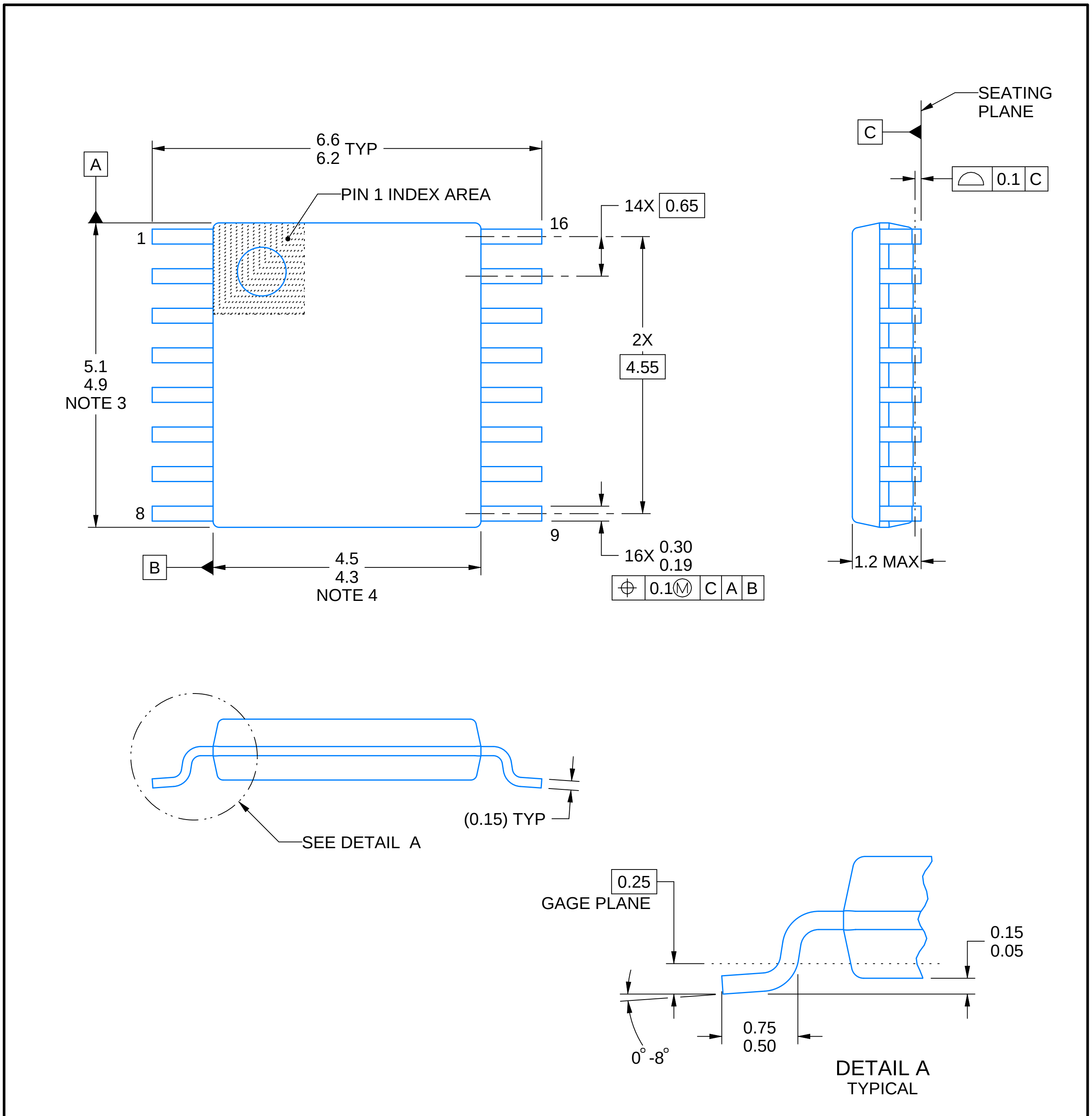


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16) PLASTIC SMALL OUTLINE



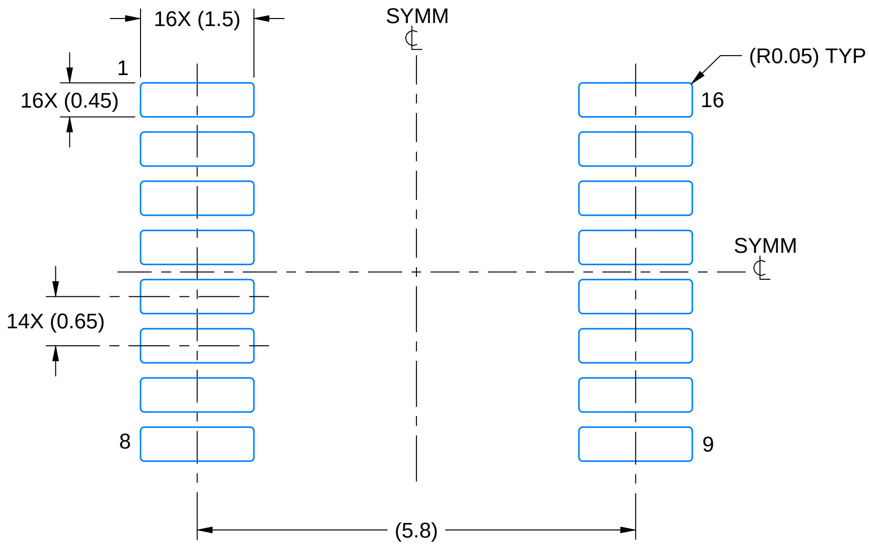
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



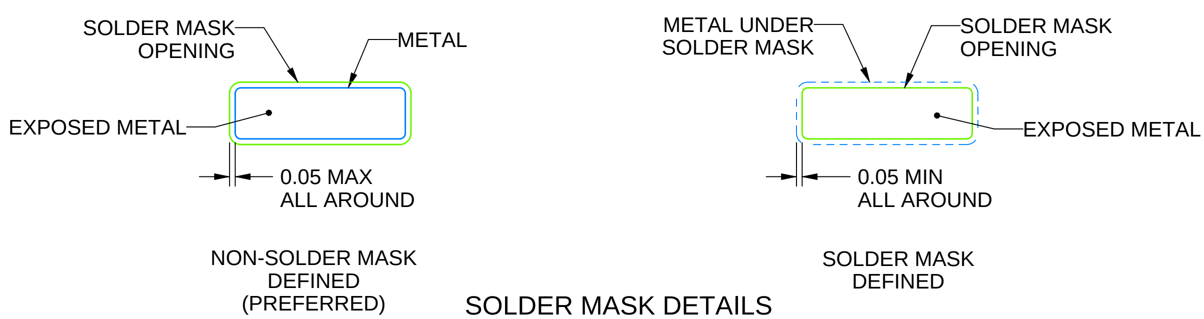
4220204/A 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

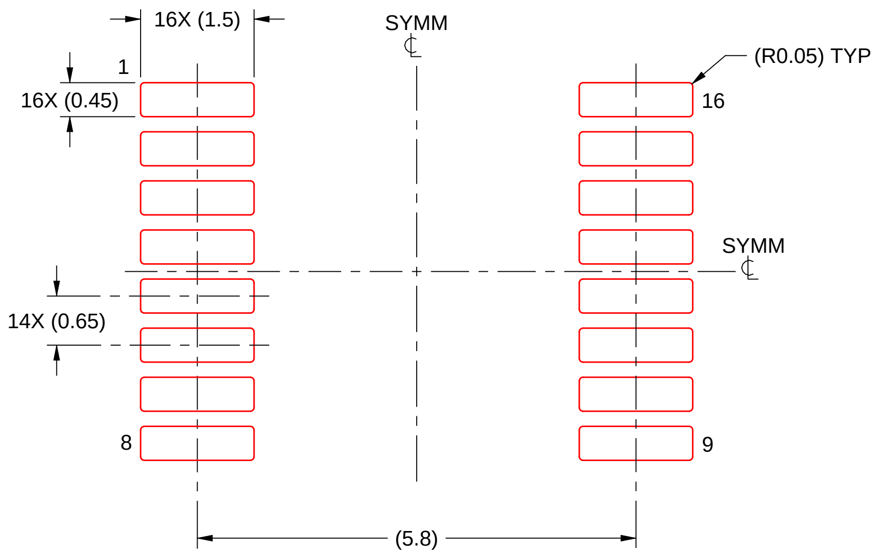


SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

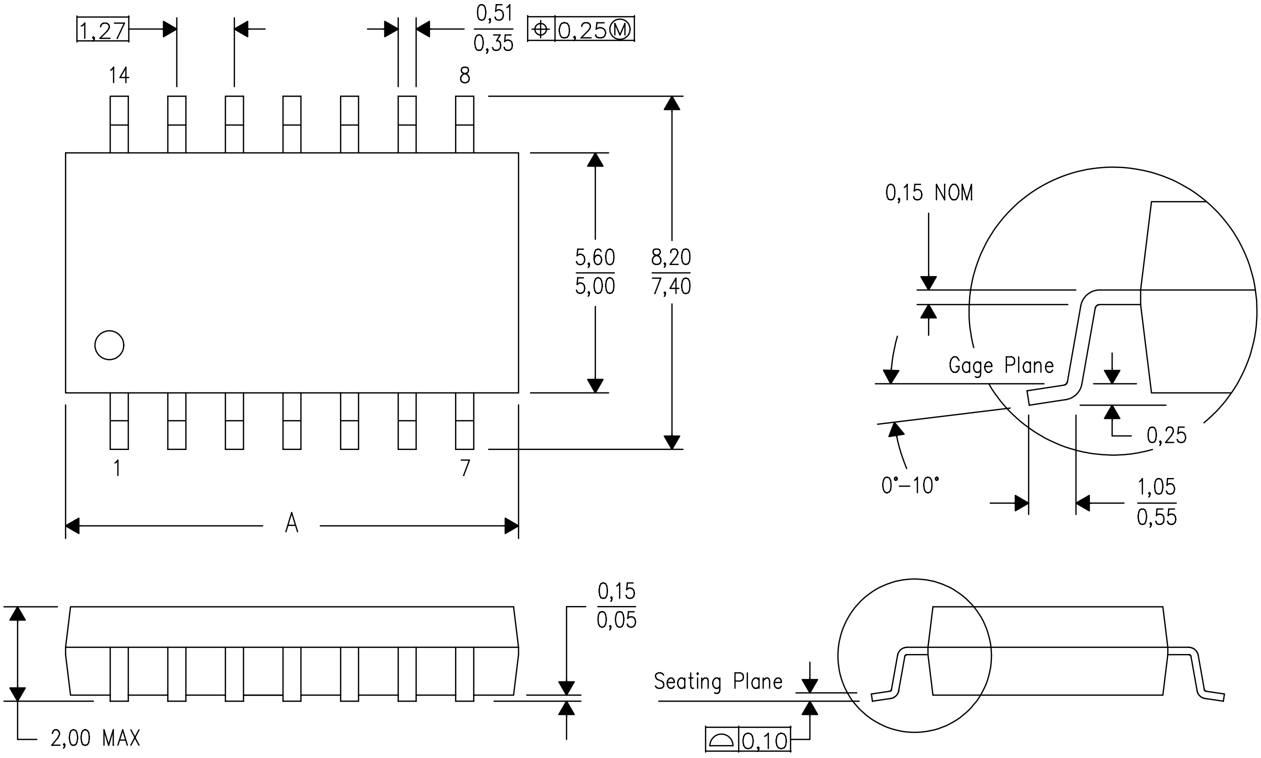
4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



PINS ** / DIM	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265