VL53L7CH

Datasheet

Artificial intelligence enabler, Time-of-Flight (ToF) 8x8 multizone sensor with 90° FoV

Product status link
VL53L7CH

Features

- Compact and normalized histogram (CNH) data output for AI
  - Multizone data output up to 64 separate zones
  - Histogram output with signal count for each bin
  - Histogram size programmable up to 128 bins
  - Minimum bin width down to 37 mm
  - Maximum frequency up to 30 Hz through I²C
  - Ambient IR light level reported for each zone
  - All Time-of-Flight (ToF) processed data (distance, signal amplitude, reflectance etc...) are available, in addition to CNH
- Highly configurable CNH in order to meet user expectations
  - 64 zones with 18 bins at 15 Hz
  - 32 zones with 36 bins at 15 Hz
  - 16 zones with 48 bins at 25 Hz
- Ultrawide ToF sensor with 90° field of view (FoV)
  - 60° x 60° square FoV (90° diagonal)
  - Autonomous low-power mode with interrupt programmable thresholds to wake up the host
  - Up to 350 cm ranging
  - Motion indicator for each zone to detect if targets have moved and how they have moved
- Fully integrated miniature module
  - Emitter: 940 nm invisible light vertical cavity surface emitting laser (VCSEL)
  - Diffractive optical elements (DOE) on both transmitter and receiver enabling square FoV
  - Receiving array of single photon avalanche diodes (SPADs)
  - Low-power microcontroller running firmware
  - Size: 6.4 x 3.0 x 1.6 mm
- Easy integration
  - Single reflowable component
  - Flexible power supply options, single 3.3 V or 2.8 V operation, or combination of either 3.3 V or 2.8 V AVDD with 1.8 V IOVDD
  - Compatible with wide range of cover glass materials
  - Driver compatible with VL53L8CH
  - Pin-to-pin compatible with VL53L5CX and VL53L7CX

Application

- AI applications requiring multizone raw data
- Cup rim detection for coffee machine and beverage dispenser
- Floor sensing for robotics and vacuum cleaners
- Gesture motion and hand posture recognition
- People counting for smart building and smart home

Description

The VL53L7CH is the perfect Time-of-Flight sensor enabling AI applications, with ultrawide 90° diagonal FoV and low power consumption. The compact and normalized histogram (CNH) innovative data output is specially designed for artificial intelligence (AI) applications requiring multizone raw data from a high performance multizone ToF sensor.

The IR signal measured in each zone is sent as raw data to the host through each bin of the histogram. Highly configurable, the user can program the resolution of the VL53L7CH up to 64 zones (8x8 zones), modify the histogram resolution up to 128 bins, and define the bin width. All this CNH data is transmitted to the host through I²C, up to 30 Hz, in addition to the standard processed data of the ToF sensor (ranging distance, signal level, reflectance etc.).

The CNH data transform ST Time-of-Flight ranging sensor into a versatile optical sensor, which can enable endless AI-based applications. This CNH raw data sent to the host, on top of the standard ranging data, opens the door to many new applications beyond simple distance measurements. From solid material (carpet, wood, glass, mirror...) to gas or liquid (water, oil, chemical...), it becomes possible to detect the location and the size of a cup in a coffee machine or beverage dispenser, to sense the floor material for robotics, and develop advanced shape, motion, or hand posture recognition.

The VL53L7CH Time-of-Flight sensor offers an ultrawide 90° diagonal FoV, shaped as a square 60° x 60° FoV, thanks to the innovative metalens surface ODIF lenses. The integrated VCSEL emits fully invisible 940 nm IR light, which is Class 1 certified and safe for the eyes.

1 Acronyms and abbreviations

Acronym/abbreviation	Definition
AF	autofocus
API	application programming interface
AR/VR	augmented reality/virtual reality
CNH	compact normalized histogram
DOE	diffractive optical element
ESD	electrostatic discharge
FoV	field of view
FoI	field of illumination
GPIO	general-purpose input/output
HP	high power
I^2C	inter-integrated circuit (serial bus)
LAF	laser autofocus
LGA	land grid array
LP	low power
NVM	nonvolatile memory
PCB	printed circuit board
PDAF	phase detection autofocus
PLL	phase-locked loop
PVT	process, voltage and temperature
POR	power on reset
RAM	random access memory
SPAD	single photon avalanche diode
SW	software
ToF	Time-of-Flight
UI	user interface
UM	user manual
VCSEL	vertical cavity surface emitting laser

2 Product overview

2.1 Technical specifications

Table 1. **Technical specifications**

Feature	Details
Package	Optical LGA16
Size	6.4 x 3.0 x 1.6 mm
Ranging	2 to 350 cm per zone
Operating voltage	IOVDD: 1.8 or 2.8 V or 3.3 V AVDD: 2.8 V or 3.3 V
Operating temperature	-30 to 85°C
Sample rate	Up to 60 Hz
Infrared emitter	940 nm
I^2C interface	I^2C: serial bus, address: 0x52
Operating ranging mode	Continuous or Autonomous (see UM3183 for more information)

2.2 Field of view

Rx (or collector) exclusion zone includes all modules assembly tolerances and is used to define the cover glass dimensions. The cover glass opening must be equal to or wider than the exclusion zone.

The detection volume represents the applicative or system FoV in which a target is detected, and a distance measured. It is determined by the Rx lens or the Rx aperture, and is narrower than the exclusion zone.

Figure 1. **System FoV and exclusion zone description (not to scale)**

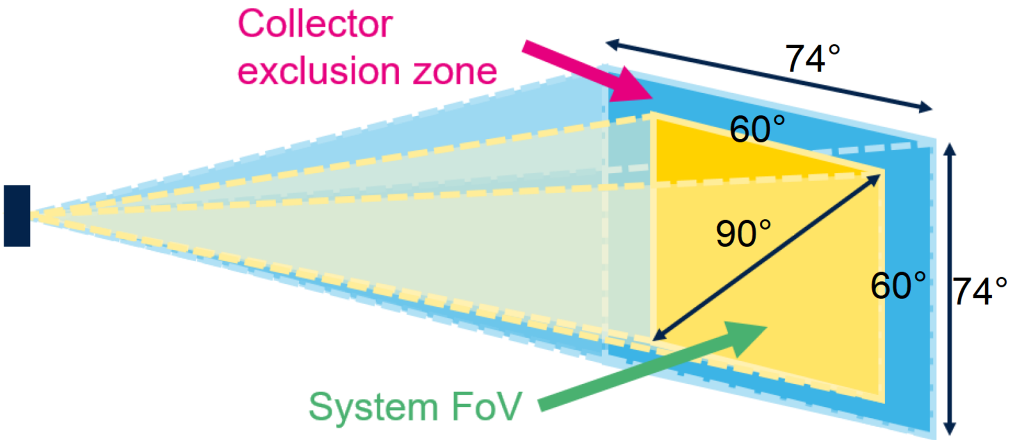


Table 2. **FoV angles**

	Horizontal	Vertical	Diagonal
Detection volume	60º	60º	90º
Collector exclusion zone	74º	74º	105º

Note: Detection volume depends on the environment and sensor configuration as well as target distance, reflectance, ambient light level, sensor resolution, sharpener, ranging mode, and integration time.

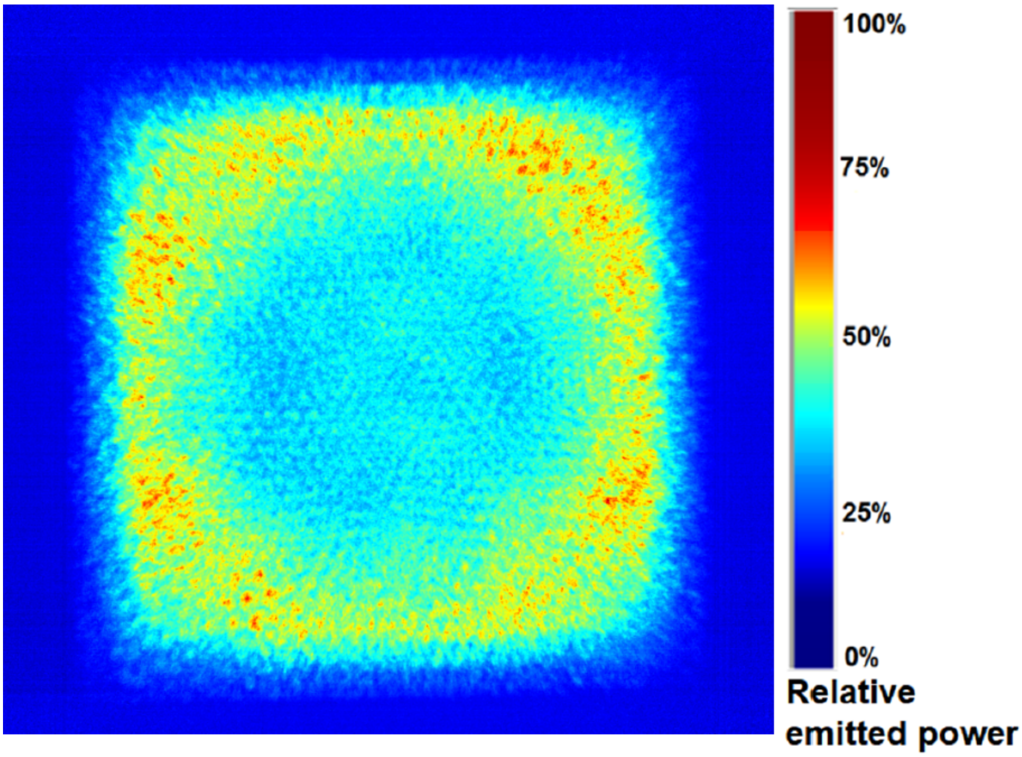
Note: *The detection volume of Table 2. FoV angles has been measured with a white 88% reflectance perpendicular target in full FoV, located at 1 m from the sensor, without ambient light (dark conditions), with an 8x8 resolution and 14% sharpener (default value), in continuous mode at 15 Hz.*

2.3 Field of illumination

The VCSEL field of illumination (FoI) is shown in the figure below. The relative emitted signal power depends on the FoI angle, and corresponds to:

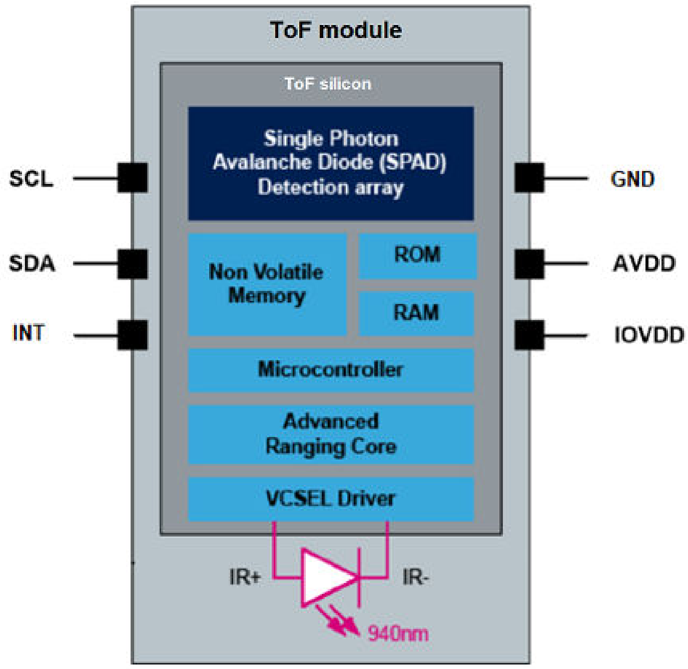
- 73.8° x 73.8° considering a beam with 75% signal from maximum
- 80.8° x 80.8° considering a beam with 10% signal from maximum

Figure 2. VL53L7CH FoI



2.4 System block diagram

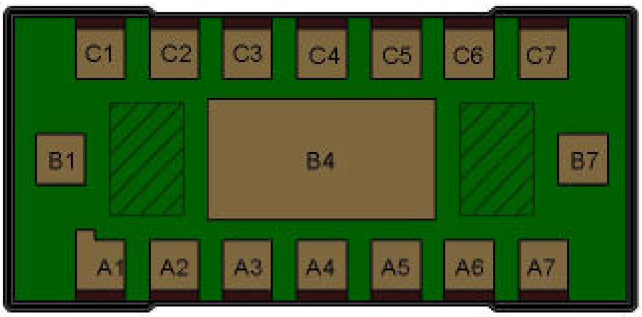
Figure 3. **VL53L7CH block diagram**



2.5 Device pinout

The figure below shows the pinout of the VL53L7CH.

Figure 4. **VL53L7CH pinout (bottom view)**



The VL53L7CH pin description is given in the table below.

Table 3. VL53L7CH pin description

Pin number	Signal name	Signal type	Signal description
A1	I2C_RST	Digital input	I^2C interface reset pin, active high. Toggle this pin from 0 to 1, then back to 0 to reset the I^2C target. Connect to GND via 47 kΩ resistor.
A2	RSVD4	Reserved	Connect to ground
A3	INT	Digital input/output (I/O)	Interrupt output, defaults to opendrain output (tristate), 47 kΩ pullup resistor to IOVDD required
A4	IOVDD	Power	1.8 V, 2.8 V or 3.3 V supply for digital core and I/O supply
A5	LPn	Digital input	Comms enable. Drive this pin to logic 0 to disable the I^2C comms when the device is in LP mode. Drive this pin to logic 1 to enable I^2C comms in LP mode. Typically used when it is required to change the I^2C adress in multidevice systems. A 47 kΩ pullup resistor to IOVDD is required.
A6	RSVD1	Reserved	Connect to ground
A7	RSVD2	Reserved	Connect to ground
B1	AVDD	Power	2.8 V or 3.3 V analog and VCSEL supply
B4	THERMALPAD	Ground	Connect to a ground plane to allow good thermal conduction
B7	AVDD	Power	2.8 V or 3.3 V analog and VCSEL supply
C1	GND	Ground	Ground
C2	RSVD6	Reserved	General purpose I/O, defaults to opendrain output (tristate), 47 kΩ pullup resistor to IOVDD required
C3	SDA	Digital I/O	Data (bidirectional), 2.2 kΩ pullup resistor to IOVDD required
C4	SCL	Digital input	Clock (input), 2.2 kΩ pullup resistor to IOVDD required
C5	RSVD5	Reserved	Do not connect
C6	RSVD3	Reserved	Connect to ground
C7	GND	Ground	Ground

Note: The THERMALPAD pin has to be connected to ground (for more information refer to AN5853).

Note: All digital signals must be driven to the IOVDD level.

Note: Toggling the I2C_RST pin resets the sensor I2C communication only. It does not reset the sensor itself. To reset the sensor refer to the sensor reset management procedure (UM3183).

2.6 Application schematic

The figures below show the application schematic of the VL53L7CH with different IOVDD and AVDD combinations.

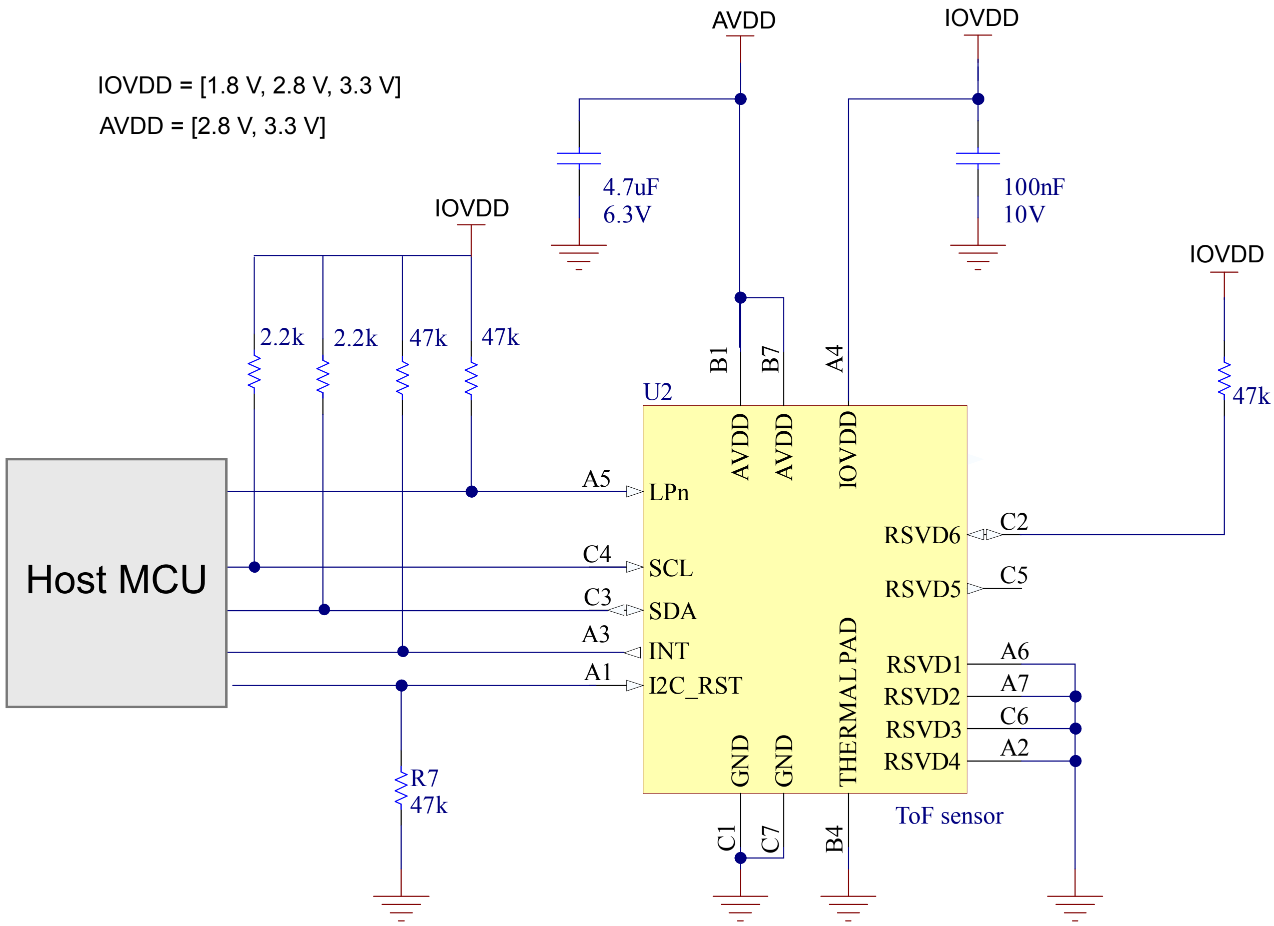


Figure 5. **Typical application schematic**

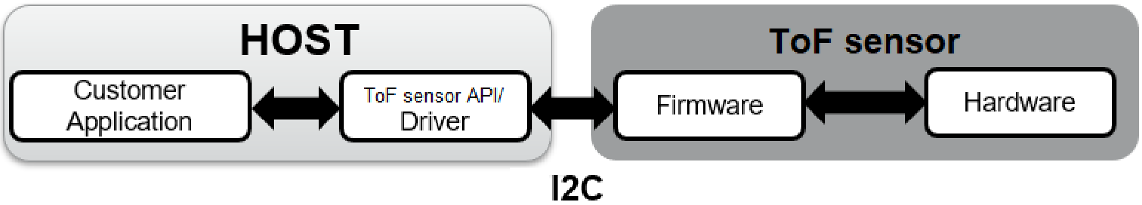
Note: Capacitors on the external supplies (AVDD and IOVDD) should be placed as close as possible to the module pins.

3 Functional description

3.1 Software interface

This section shows the software interface of the device. The host customer application controls the VL53L7CH using an application programming interface (API). The API implementation is delivered to the customer as a driver (C code and reference Linux® driver). The driver provides the customer application with a set of high level functions that allow control of the VL53L7CH firmware such as device initialization, ranging start/stop, mode select etc.

Figure 6. VL53L7CH system functional description



3.2 Power state machine

Figure 7. Power state machine

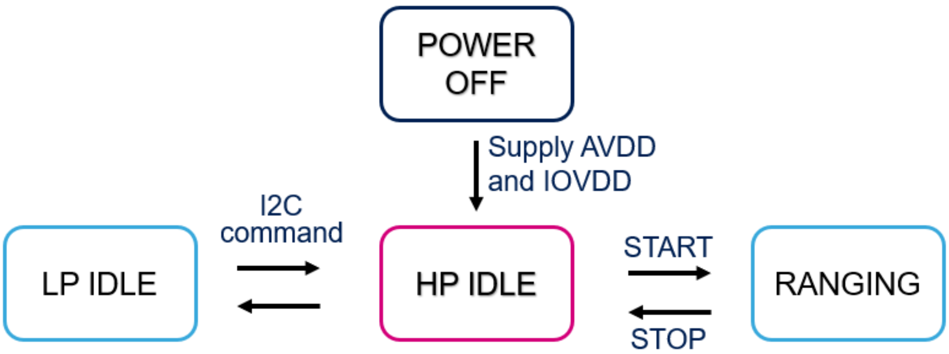


Table 4. Power state description

Device state	Description
LP idle	Low power idle state with data retention RAM and register content retained Allows fast resume to HP idle I^2C communication disabled if using LPn
HP idle	High power idle state Device needs to be in HP idle state to start ranging Power up state
Ranging	Full operation VCSEL is active (pulsing)

3.3 Power up sequence

The recommended power up sequence is shown in the figure below. When powering up the device, the IOVDD supply should be applied at the same time or after AVDD. When removing power, the AVDD supply should be removed at the same time or after IOVDD.

Note: Avoid powering IOVDD while AVDD is unpowered to prevent increased leakage current.

Figure 8. Power up sequence

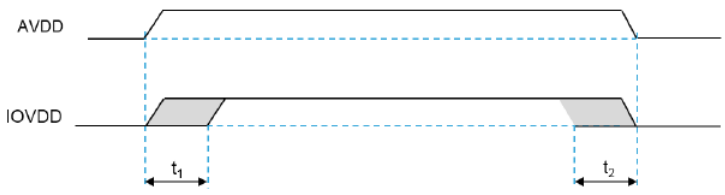


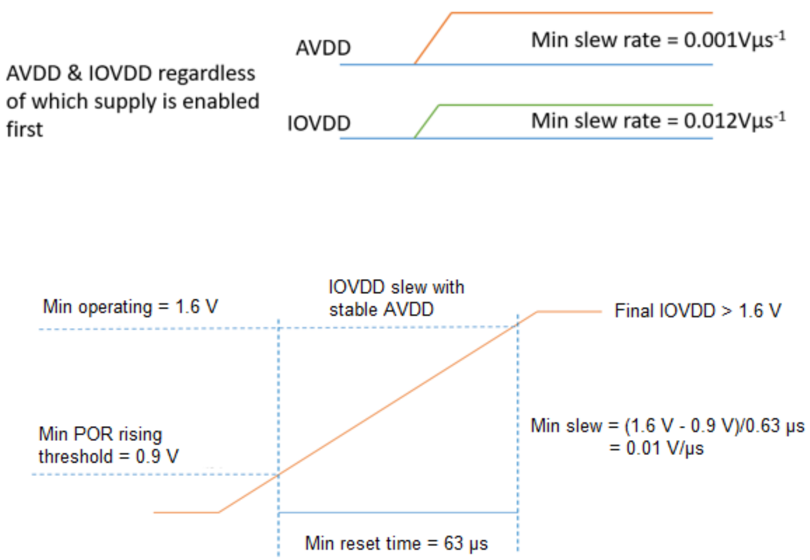
Table 5. Power up timing table

Time	Description	Min.
t_1	IOVDD rise after AVDD	0 s
t_2	IOVDD fall before AVDD	0 s

3.3.1 Power up slew

To ensure proper operation of the module, the following minimum slew rates on the supplies must be met for correct operation of the power on reset (POR) circuitry. The POR circuitry triggers at 0.9 V, but the supplies should reach their operation levels in accordance with the slew rates listed in the table below.

Figure 9. Power up slew



Note: The minimum reset time is the minimum time required for the device ROM to load and boot up after IOVDD reaches the POR rising threshold. The supply must have reached the minimum operating level (1.6 V) within this time.

Note: The minimum slew rate on the IOVDD is the same regardless of 1.8 V or 2.8 V operation.

Note: The AVDD rise time is determined by the internal analogue levels which must be stable for correct operation.

Table 6. Supply slew rate minimum limits

Supply status	AVDD slew	IOVDD slew
Start together	0.001 V/µs	0.012 V/µs
AVDD stable followed by IOVDD	—	0.012 V/µs
IOVDD stable followed by AVDD	0.001 V/µs	—

3.3.2 Power up and I²C access

For correct operation of the device, the I²C interface assumes the power level has reached 1.62 V.

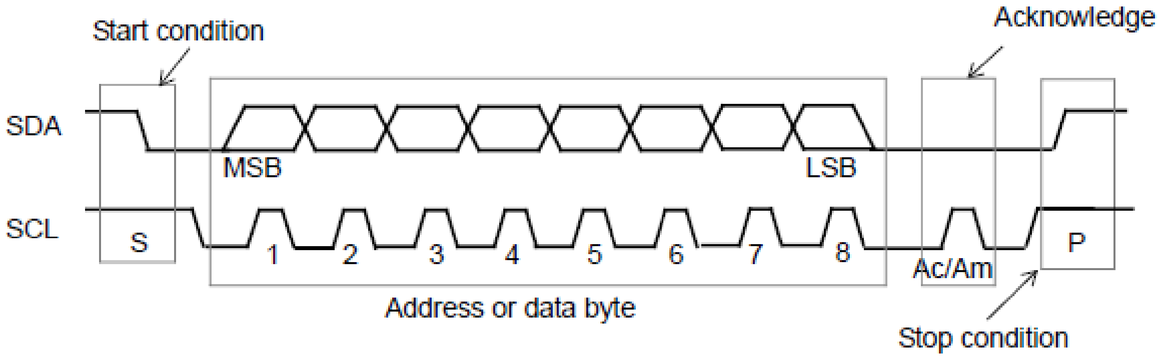
4 I^2C control interface

This section specifies the control interface. The I^2C interface uses two signals: serial data line (SDA) and serial clock line (SCL). Each device connected to the bus uses a unique address and a simple controller/target relationships exists.

Both SDA and SCL lines are connected to a positive supply voltage using pull-up resistors located on the host. Lines are only actively driven low. A high condition occurs when lines are floating and the pull-up resistors pull lines up. When no data is transmitted both lines are high.

Clock signal (SCL) generation is performed by the controller device. The controller device initiates data transfer. The I^2C bus on the VL53L7CH has a maximum speed of 1 Mbits/s and uses a device 8-bit address of 0x52.

Figure 10. Data transfer protocol



Information is packed in 8-bit packets (bytes) always followed by an acknowledge bit, Ac for VL53L7CH acknowledge and Am for controller acknowledge (host bus controller). The internal data are produced by sampling SDA at a rising edge of SCL. The external data must be stable during the high period of SCL. The exceptions to this are start (S) or stop (P) conditions when SDA falls or rises respectively, while SCL is high.

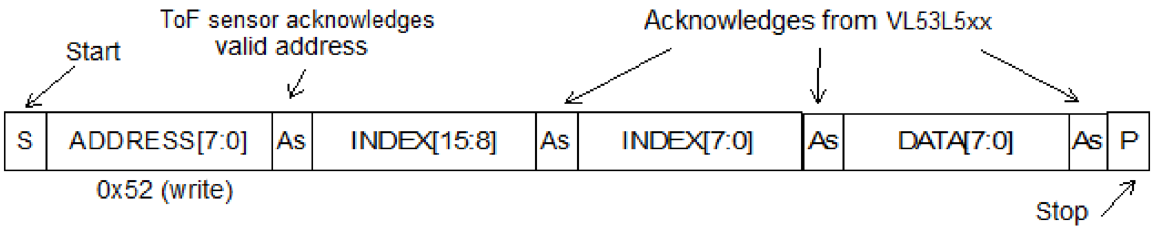
A message contains a series of bytes preceded by a start condition and followed by either a stop or repeated start (another start condition but without a preceding stop condition) followed by another message. The first byte contains the device address (0x52) and also specifies the data direction. If the least significant bit is low (that is, 0x52) the message is a controller-write-to-the-target. If the lsb is set (that is, 0x53) then the message is a controller-read-from-the-target.

Figure 11. VL53L7CH I^2C device address: 0x52

MSBit							LSBit
0	1	0	1	0	0	1	R/W

All serial interface communications with the ToF sensor must begin with a start condition. The VL53L7CH module acknowledges the receipt of a valid address by driving the SDA wire low. The state of the read/write bit (lsb of the address byte) is stored and the next byte of data, sampled from SDA, can be interpreted. During a write sequence, the second byte received provides a 16-bit index, which points to one of the internal 8-bit registers.

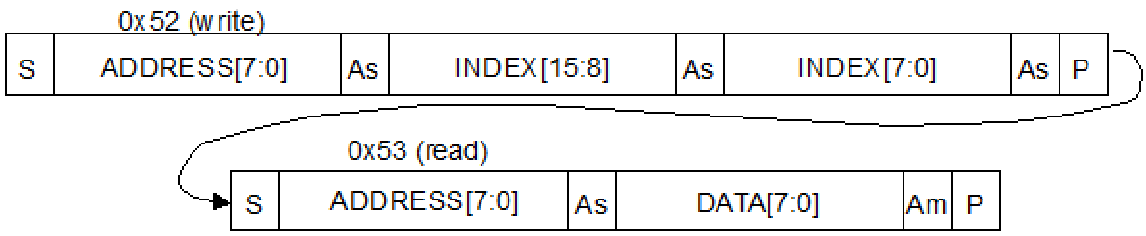
Figure 12. **VL53L7CH data format (write)**



As data are received by the target, they are written bit by bit to a serial/parallel register. After each data byte has been received by the target, an acknowledge is generated, the data are then stored in the internal register addressed by the current index.

During a read message, the contents of the register addressed by the current index is read out in the byte following the device address byte. The contents of this register are parallel loaded into the serial/parallel register and clocked out of the device by the falling edge of SCL.

Figure 13. **VL53L7CH data format (read)**



At the end of each byte, in both read and write message sequences, an acknowledge is issued by the receiving device (that is, the VL53L7CH for a write and the host for a read).

A message can only be terminated by the bus controller, either by issuing a stop condition or by a negative acknowledge (that is, not pulling the SDA line low) after reading a complete byte during a read operation.

The interface also supports auto-increment indexing. After the first data byte has been transferred, the index is automatically incremented by 1. The controller can therefore send data bytes continuously to the target until the target fails to provide an acknowledge or the controller terminates the write communication with a stop condition. If the auto-increment feature is used, the controller does **not** have to send address indexes to accompany the data bytes.

Figure 14. **VL53L7CH data format (sequential write)**

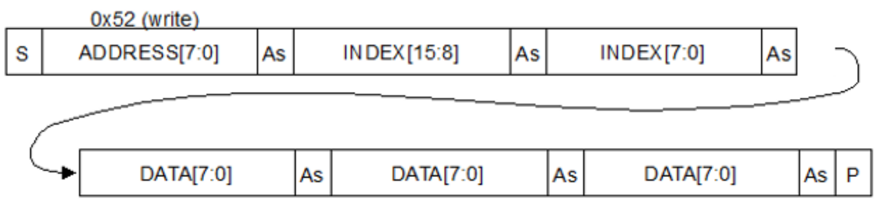
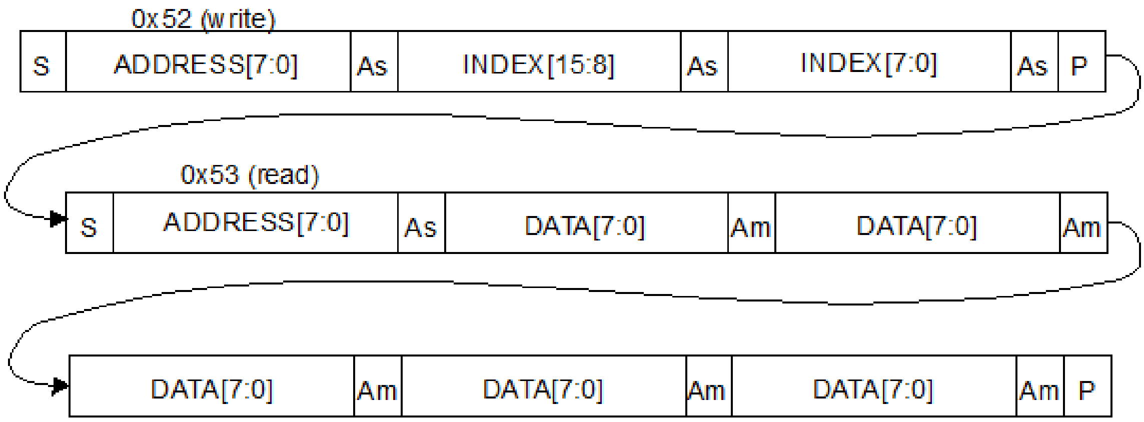


Figure 15. VL53L7CH data format (sequential read)



4.1 I²C interface - timing characteristics

Timing characteristics are shown in the tables below. Refer to the figure below for an explanation of the parameters used.

Timings are given for all process, voltage, and temperature (PVT) conditions.

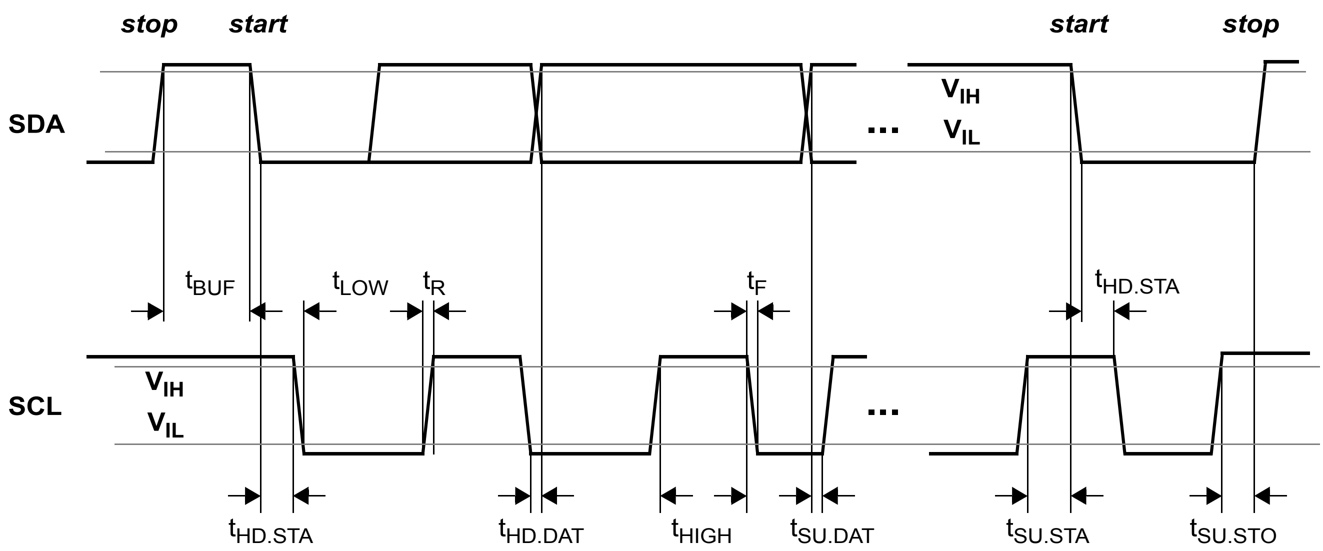
Table 7. I²C interface - timing characteristics for fast mode plus (1 MHz)

Symbol	Parameter	Minimum	Typical	Maximum	Unit
F_{I2C}	Operating frequency	0	—	1000	kHz
t_{LOW}	Clock pulse width low	0.5	—	—	µs
t_{HIGH}	Clock pulse width high	0.26	—	—	µs
t_{SP}	Pulse width of spikes, which are suppressed by the input filter	—	—	50	ns
t_{BUF}	Bus free time between transmissions	0.5	—	—	µs
$t_{HD.STA}$	Start hold time	0.26	—	—	µs
$t_{SU.STA}$	Start setup time	0.26	—	—	µs
$t_{HD.DAT}$	Data in hold time	0	—	0.9	µs
$t_{SU.DAT}$	Data in setup time	50	—	—	ns
t_R	SCL/SDA rise time	—	—	120	ns
t_F	SCL/SDA fall time	—	—	120	ns
$t_{SU.STO}$	Stop setup time	0.26	—	—	µs
Ci/o	Input/output capacitance (SDA)	—	—	10	pF
Cin	Input capacitance (SCL)	—	—	4	pF
C_L	Load capacitance	—	140	550	pF

Table 8. I²C interface - timing characteristics for fast mode (400 kHz)

Symbol	Parameter	Minimum	Typical	Maximum	Unit
F_{I2C}	Operating frequency	0	—	400	kHz
t_{LOW}	Clock pulse width low	1.3	—	—	µs
t_{HIGH}	Clock pulse width high	0.6	—	—	µs
t_{SP}	Pulse width of spikes which are suppressed by the input filter	—	—	50	ns
t_{BUF}	Bus free time between transmissions	1.3	—	—	µs
$t_{HD.STA}$	Start hold time	0.26	—	—	µs
$t_{SU.STA}$	Start setup time	0.26	—	—	µs
$t_{HD.DAT}$	Data in hold time	0	—	0.9	µs
$t_{SU.DAT}$	Data in setup time	50	—	—	ns
t_R	SCL/SDA rise time	—	—	300	ns
t_F	SCL/SDA fall time	—	—	300	ns
$t_{SU.STO}$	Stop setup time	0.6	—	—	µs
Ci/o	Input/output capacitance (SDA)	—	—	10	pF
Cin	Input capacitance (SCL)	—	—	4	pF
C_L	Load capacitance	—	125	400	pF

Figure 16. I²C timing characteristics



5 Electrical characteristics

5.1 Absolute maximum ratings

Table 9. Absolute maximum ratings

Parameter	Min.	Typ.	Max.	Unit
AVDD, IOVDD	-0.5	—	3.6	V
SCL, SDA, LPn, INT, and I2C_RST	-0.5	—	3.6	

Note: Stresses above those listed in Section 2 Product overview may cause permanent damage to the device. This is a stress rating only. Functional operation of the device is not implied at these, or any other conditions above those indicated in the operational sections of the specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

5.2 Recommended operating conditions

Table 10. Recommended operating conditions

Parameter		Min.	Typ.	Max.	Unit
AVDD supply(1)	2.8 V configuration	2.5	2.8	3.3	V
	3.3 V configuration	3.0	3.3	3.6	
IOVDD supply	1.8 V configuration	1.62	1.8	1.98	
	2.8 V configuration	2.5	2.8	3.3	
	3.3 V configuration	3.0	3.3	3.6	
Ambient temperature (normal operating)		-30	—	85	°C

1. *AVDD is independent of IOVDD*

5.3 Electrostatic discharge (ESD)

The VL53L7CH is compliant with the ESD values presented in the table below.

Table 11. ESD performances

Parameter	Specification	Conditions
Human body model	JEDEC JS-001-2014	± 2 kV, 1500 Ohms, 100 pF
Charged device model	JEDEC JS-002-2014	± 500 V

5.4 Current consumption

The current consumption values are given in the table below.

- Typical values quoted are for nominal voltage, process, and temperature (23°C).
- Maximum values are quoted for worst case conditions (process, voltage, and temperature) unless stated otherwise (70°C).

Table 12. Current consumption

Device State	Average current consumption				Unit
	AVDD		IOVDD		
	Typ.	Max.	Typ.	Max.	
LP idle	45	300	0.1	1	µA
HP idle	1.3	1.6	2.8	35	mA
Active ranging[1]	45	50	50	80	mA

1. *Active ranging is when the device is actively ranging. The current consumption is not affected by 4x4 or 8x8 zone configuration*

IOVDD peak current is the average value +10 mA.

AVDD peak current is the average current +10 mA.

Table 13. Example of typical power consumption in continuous mode

Parameter	2V8/1V8	2V8/2V8	3V3/3V3	Unit
Continuous mode (4x4 mode or 8x8 mode)	216	266	313	mW

Table 14. Example of typical power consumption in autonomous mode

Parameter	2V8/1V8	2V8/2V8	3V3/3V3	Unit
4x4 mode - 1 Hz frame rate with 20 ms integration time	5.4	6.7	8.3	mW
4x4 mode - 5 Hz frame rate with 20 ms integration time	25	31	39	
8x8 mode - 1 Hz frame rate with 20 ms integration time	19	24	29	
8x8 mode - 5 Hz frame rate with 20 ms integration time	88	112	135	

5.5 Digital input and output

The following tables summarize the digital I/O electrical characteristics.

Table 15. INT, I2C_RST, LPn

Symbol	Parameter	IOVDD configuration	Min.	Max.	Unit
V_{IL}	Low level input voltage	1.8 V	-0.3	0.35* IOVDD	V
		2.8 V - 3.3 V			
V_{IH}	High level input voltage	1.8 V	0.65*IOVDD	2.28	
		2.8 V - 3.3 V		3.6	
V_{OL}	Low level output voltage (I_{OUT} = 4 mA)	1.8 V	—	0.4	
		2.8 V - 3.3 V			
V_{OH}	High level output voltage (I_{OUT} = 4 mA)	1.8 V	1.22	—	
		2.8 V - 3.3 V	2.1		

Table 16. I²C interface (SDA/SCL)

Symbol	Parameter	IOVDD configuration	Min.	Max.	Unit
V_{IL}	Low level input voltage	1.8 V	-0.3	0.54	V
		2.8 V - 3.3 V		0.3*IOVDD	
V_{IH}	High level input voltage	1.8 V	1.13	2.28	
		2.8 V - 3.3 V		3.6	
V_{OL}	Low level output voltage (I_{out} = 4 mA)	1.8 V	—	0.4	
		2.8 V- 3.3 V			
$I_{IL/IH}$	Leakage from IOVDD supply		—	2.5	µA
	Leakage from IOVDD pad		—	1	

Note: I²C pads use 1V8 switching thresholds for all IOVDD supplies.

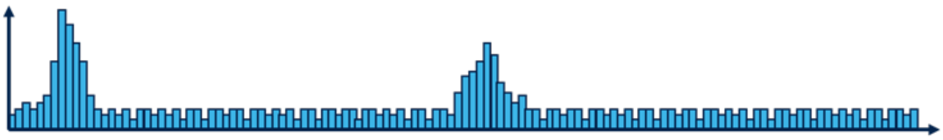
Note: A maximum load of 12 mA is assumed in the above table.

6 Histogram (CNH) output

Up to 6 KB of histogram data can be read by the host at every frame. Selection of what histogram data is placed in this 6 KB data area is highly configurable, allowing the amount of the data transferred to be optimized for different applications. The format of the collected histogram data is called compact normalized histogram (CNH):

- Compact: Options are available to reduce the amount of data compared to the native “raw” histogram data
- Normalized: Raw data are adjusted to compensate variations caused by frame-to-frame adjustments
- Histogram: Primary data is in the form of histograms recording return-signal-strength vs range

Figure 17. **Raw histogram (128 bins)**



The sensor is highly configurable: User can program the number of bins, the bins width, and also the region-of-interest. Ambient light level is measured during ranging and removed from the histogram data. A record of the ambient light level that was removed from each histogram is available in a separate area of the data result buffer.

Data aggregation options during preprocessing include region-of-interest and subsampling operations both spatially (zone based), and temporally (on histogram bins).

Table 17. **ToF ranging core histogram characteristics**

Parameter	Value	Units
Ranging core histogram bin width	250	ps
Ranging core histogram bin equivalent range	37.5	mm
Ranging core number of bins in histogram	128	bins

Table 18. **CNH (compact normalised histogram) parameters**

Setting	Value	Units
CNH buffer maximum size	6160	bytes
Bytes-per-histogram bin	5	bytes
Maximum zones per CNH aggregate	64	zones
Maximum histogram binning factor	8	—
Bytes-per-ambient level	5	bytes

Note: Details of the CNH configuration options available can be found in the user manual, document UM3183.

Table 19. **Example operating configurations**

Number of histograms	Bins per CNH histogram	CNH data size (bytes)	Transfer time (ms)	Framerate (fps)
8	80	3268	32	30
8	128	5188	48	20
16	48	3948	36	25
16	72	5868	54	18
32	36	6108	56	15
64	18	6108	56	15

Note: *Data transfer timing is for I²C interface with an SCL clock at 1 MHz. CNH data size includes histogram and ambient light level data. No per-zone target data is included in the data transfer. Details of how to configure such operating modes can be found user manual document UM3183.*

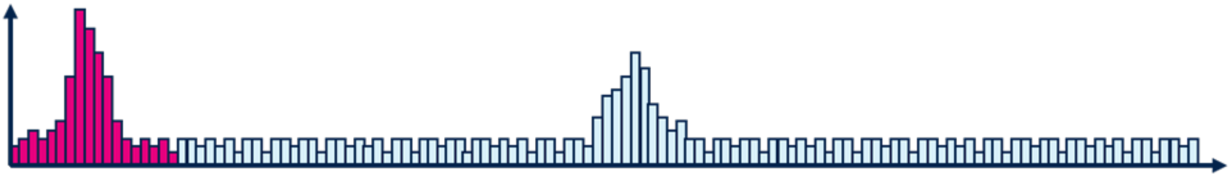


Figure 18. **CNH example 1 (18 bins selected, binning factor = 1)**

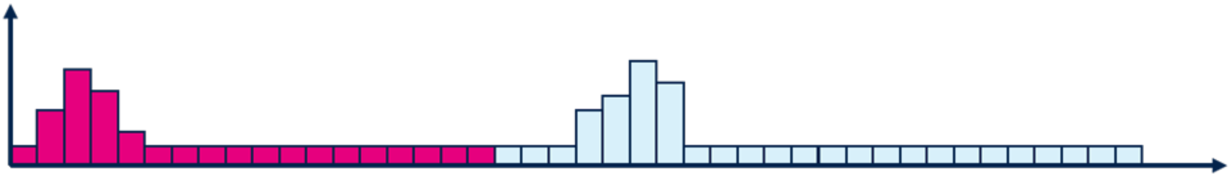


Figure 19. **CNH example 2 (18 bins selected, binning factor = 3)**

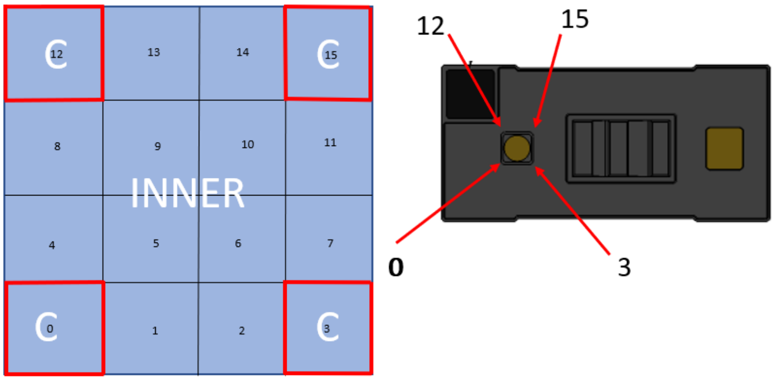
7 Ranging performance

7.1 Zone mapping

7.1.1 Zone mapping 4x4

The figure below shows the zone definition in 4x4 mode. There are 16 zones in total which increment along a row first before starting a new row. The physical view is from the device top into the lens. The number of each zone, as indicated in the figure below, corresponds to the ZoneIDs returned by the sensor.

Figure 20. Zone mapping in 4x4 mode

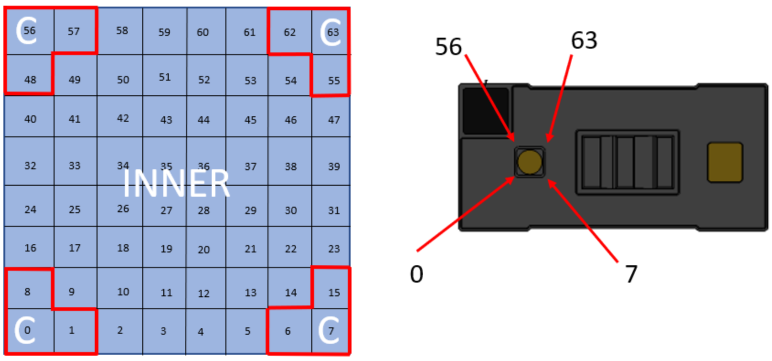


C = Corner zones
INNER = all zones not
identified as the corner

7.1.2 Zone mapping 8x8

The figure below shows the zone definition in 8x8 mode. There are 64 zones in total which increment along a row first before starting a new row. The physical view is from the device top into the lens. The number of each zone, as indicated in the figure below, correspond to the ZoneIDs returned by the sensor to the host.

Figure 21. Zone mapping in 8x8 mode

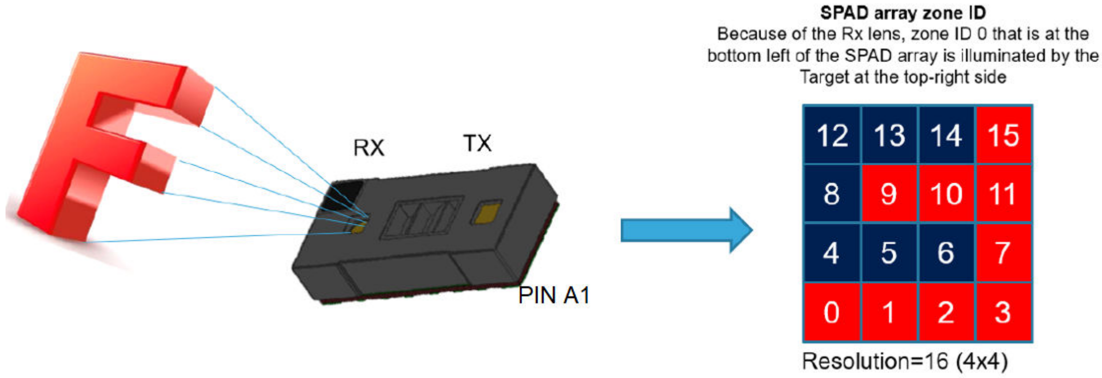


C = Corner zones
INNER = all zones not
identified as the corner

7.1.3 Effective zone orientation

The VL53L7CH module includes a lens over the Rx aperture, which flips (horizontally and vertically) the captured image of the target. Consequently, the zone identified as zone 0 in the bottom left of the SPAD array, is illuminated by a target located at the top right-hand side of the scene.

Figure 22. Effective orientation



7.2 Continuous ranging mode

7.2.1 Measurement conditions

The following criteria and test conditions apply to all the characterization results detailed in this section unless specified otherwise:

- The specified target fills 100% of the field of view of the device (in all zones).
- Targets used are Munsell N4.75 (17%) and Munsell N9.5 (88%).
- AVDD is 2.8 V. IOVDD is 1.8 V.
- Nominal ambient temperature is 23°C.
- Maximum range capability is based on a 90% detection rate [(1)].
- Range accuracy figures are based on 2.7 sigma that is, 99.3% of measurements are within the specified accuracy.
- Tests are performed in the dark and at 2 W/m^2 target illumination (940 nm). A 2 W/m^2 target irradiance at 940 nm is equivalent to 5 kLux daylight.
- All tests are performed without cover glass with a crosstalk margin set to 0 kcps.
- The sensor relies on default calibration data.
- The device is controlled through the API using the default driver settings.

1. *The detection rate is a statistical value indicating the worst case percentage of measurements that return a valid ranging. For example, taking 1000 measurements with 90% detection rate gives 900 valid distances. The 100 other distances may be outside the specification or flagged with an invalid target status.*

7.2.2 Maximum ranging distance 4x4

The table below shows the maximum ranging capability of the VL53L7CH under different conditions. Refer to Section 7.2.1 Measurement conditions for the general test conditions.

Table 20. Maximum ranging capabilities when ranging continuously at 30 Hz

Target reflectance level. Full FoV (reflectance %)	Zone	Dark	Ambient light (5 klux)
White target (88%)	Inner	Typical 3500 mm Minimum 3300 mm	Typical 650 mm Minimum 500 mm
	Corner	Typical 3500 mm Minimum 3300 mm	Typical 600 mm Minimum 600 mm
Light gray target (54%)	Inner	Typical 2800 mm Minimum 2600 mm	Typical 600 mm Minimum 600 mm
	Corner	Typical 2800 mm Minimum 2600 mm	Typical 600 mm Minimum 600 mm
Gray target (17%)	Inner	Typical 1400 mm Minimum 1300 mm	Typical 550 mm Minimum 500 mm
	Corner	Typical 1400 mm Minimum 1200 mm	Typical 500 mm Minimum 450 mm

7.2.3 Maximum ranging distance 8x8

The table below shows the maximum ranging capability of the VL53L7CH under different conditions. Refer to Section 7.2.1 Measurement conditions for the general test conditions.

Table 21. Maximum ranging capabilities when ranging continuously at 15 Hz

Target reflectance level. Full FoV (reflectance %)	Zone	Dark (0 klux)	Ambient light (5 klux)
White target (88%)	Inner	Typical 2000 mm Minimum 1700 mm	Typical 500 mm Minimum 400 mm
	Corner	Typical 1900 mm Minimum 1100 mm	Typical 500 mm Minimum 400 mm
Light gray target (54%)	Inner	Typical 1600 mm Minimum 1500 mm	Typical 400 mm Minimum 400 mm
	Corner	Typical 1600 mm Minimum 1100 mm	Typical 400 mm Minimum 400 mm
Gray target (17%)	Inner	Typical 800 mm Minimum 700 mm	Typical 350 mm Minimum 250 mm
	Corner	Typical 750 mm Minimum 450mm	Typical 250 mm Minimum 200 mm

7.2.4 Range accuracy in continuous mode

The figure below illustrates how range accuracy is defined over distance.

Figure 23. Range accuracy vs distance

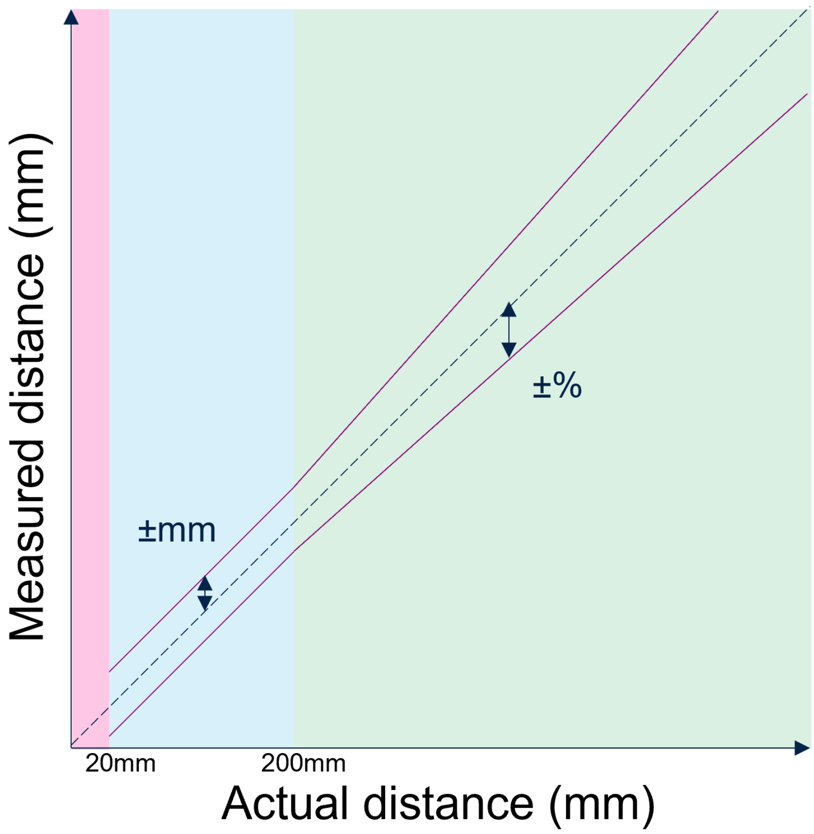


Table 22. Range accuracy in continuous mode

Mode	Distance	Target reflectance	Dark (0 klux)	Ambient light (5 klux)
4x4 (30 Hz)	20-200 mm	White target (88%)	±9 mm	±7 mm
		Light gray target (54%)	±9 mm	±7 mm
		Gray target (17%)	±10 mm	±11 mm
	200-4000 mm	White target (88%)	±3%	±7%
		Light gray target (54%)	±4%	±9%
		Gray target (17%)	±4%	±10%
8x8 (15 Hz)	20-200 mm	White target (88%)	±11 mm	±12 mm
		Light gray target (54%)	±12 mm	±14 mm
		Gray target (17%)	±12 mm	±20 mm
	200-4000 mm	White target (88%)	±5%	±9%
		Light gray target (54%)	±6%	±12%
		Gray target (17%)	±6%	±14%

7.3 Autonomous ranging mode

7.3.1 Measurement conditions

The following criteria and test conditions apply to all the characterization results detailed in this section unless specified otherwise:

- The specified target fills 100% of the field of view of the device (in all zones).
- Targets used are Munsell N4.75 (17%) and Munsell N9.5 (88%).
- AVDD is 2.8 V. IOVDD is 1.8 V.
- Nominal ambient temperature is 23°C.
- Maximum range capability is based on a 90 % detection rate (1).
- Range accuracy figures are based on 2.7 sigma that is, 99.3% of measurements are within the specified accuracy.
- Tests are performed in the dark and at 2 W/m^2 target illumination (940 nm). A 2 W/m^2 target irradiance at 940 nm is equivalent to 5 kLux daylight.
- All tests are performed without cover glass with crosstalk margin set to 0 kcps.
- The sensor relies on default calibration data.
- The device is controlled thought the API using the default driver settings.

1. *The detection rate is a statistical value indicating the worst case percentage of measurements that return a valid ranging. For example, taking 1000 measurements with 90 % detection rate gives 900 valid distances. The 100 other distances may be outside the specification or flagged with an invalid target status.*

7.3.2 Maximum ranging distance 4x4

The table below shows the maximum ranging capability of the VL53L7CH under different conditions. Refer to Section 7.3.1 Measurement conditions for the general test conditions.

Table 23. Maximum ranging capabilities when ranging with autonomous mode at 1 Hz, 4x4, integration time 20 ms

Target reflectance	Zone	Dark (0 klux)	Ambient light (5 klux)
White target (88%)	Inner	Typical: 3300 mm Minimum: 3200 mm	Typical: 650 mm Minimum: 600 mm
	Corner	Typical: 3400 mm Minimum: 3000 mm	Typical: 600 mm Minimum: 600 mm
Light gray target (54%)	Inner	Typical: 2750 mm Minimum: 2700 mm	Typical: 600 mm Minimum: 600 mm
	Corner	Typical: 2750 mm Minimum: 2500 mm	Typical: 600 mm Minimum: 550 mm
Gray target (17%)	Inner	Typical: 1250 mm Minimum: 1200 mm	Typical: 500 mm Minimum: 500 mm
	Corner	Typical: 1250 mm Minimum: 1150 mm	Typical: 500 mm Minimum: 500 mm

The table below shows the maximum ranging capability of the VL53L7CH under different conditions. Refer to Section 7.3.1 Measurement conditions for the general test conditions.

Table 24. **Maximum ranging capabilities when ranging with autonomous mode at 1 Hz, 8x8, integration time 20 ms**

Target reflectance level. Full FoV (reflectance %)	Zone	Dark (0 klux)	Ambient light (5 klux)
White target (88%)	Inner	Typical: 2000 mm Minimum: 1800 mm	Typical: 550 mm Minimum: 500 mm
	Corner	Typical: 1900 mm Minimum: 1200 mm	Typical: 550 mm Minimum: 500 mm
Light gray target (54%)	Inner	Typical: 1700 mm Minimum: 1500 mm	Typical: 500 mm Minimum: 500 mm
	Corner	Typical: 1400 mm Minimum: 1000 mm	Typical: 500 mm Minimum: 500 mm
Gray target (17%)	Inner	Typical: 800 mm Minimum: 800 mm	Typical: 500 mm Minimum: 450 mm
	Corner	Typical: 950 mm Minimum: 850 mm	Typical: 400 mm Minimum: 400 mm

7.3.3 Range accuracy - autonomous mode

Table 25. **Range accuracy – autonomous mode**

Distance (mm)	Mode	Reflectance	Dark (0 klux)	Ambient light (5 klux)
4x4, 1 Hz, 20 ms integration time	20-200 mm	White target (88%)	±10 mm	±9 mm
		Light gray target (54%)	±10 mm	±9 mm
		Gray target (17%)	±11 mm	±13 mm
	200-4000 mm	White target (88%)	±4%	±6%
		Light gray target (54%)	±3%	±5%
		Gray target (17%)	±5%	±9%
8x8, 1 Hz, 20 ms integration time	20-200 mm	White target (88%)	±12 mm	±14 mm
		Light gray target (54%)	±12 mm	±18 mm
		Gray target (17%)	±14 mm	±21 mm
	200-4000 mm	White target (88%)	±6%	±7%
		Light gray target (54%)	±6%	±8%
		Gray target (17%)	±7%	±14%

7.4 Range offset drift over temperature

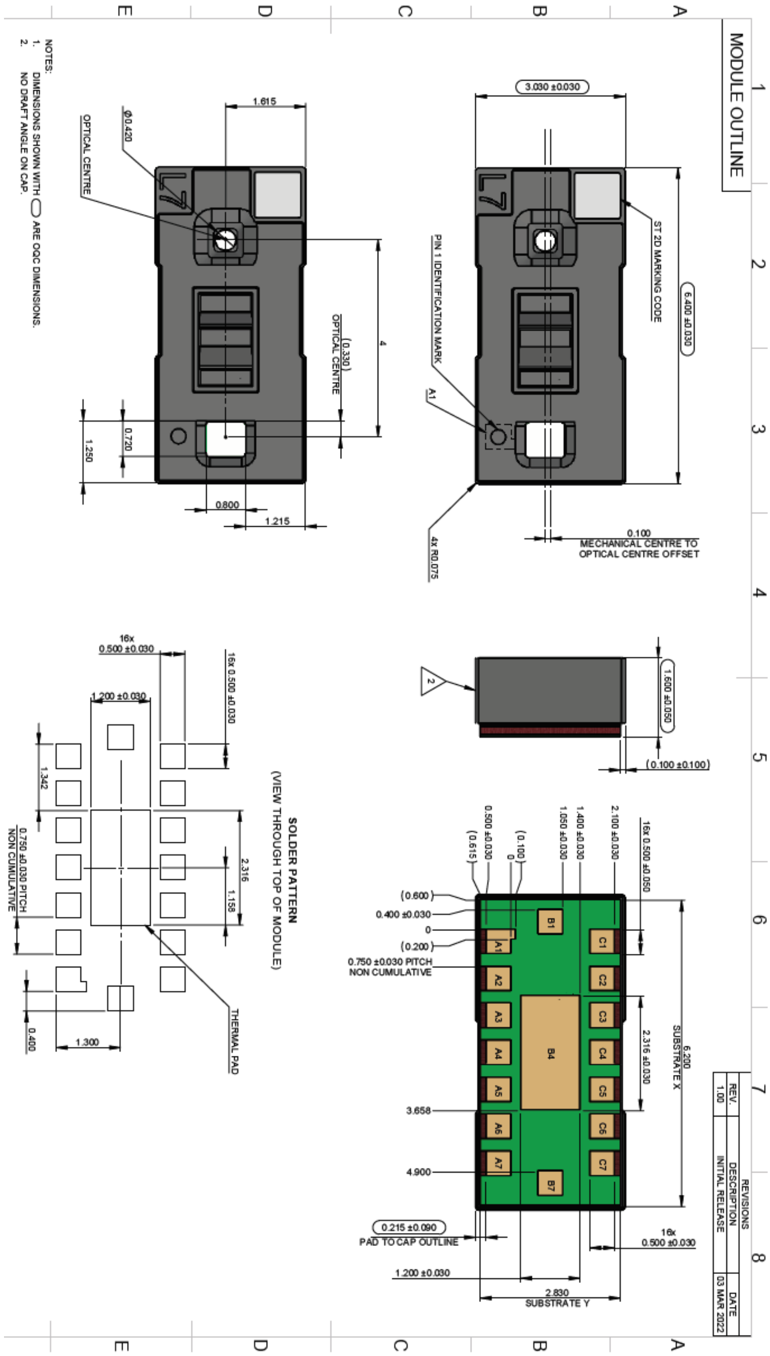
Selfheating or a change in ambient temperature increases silicon temperature, which results in a range offset drift. This may be minimized by performing a periodic autocalibration, resulting in a typical drift of 0.15 mm/°C.

The autocalibration is done automatically when a new ranging session is started. A stop/start of the device is required if the device is already streaming.

8 Outline drawings

The figures below give details of the VL53L7CH module. All values are given in millimeters.

Figure 24. Outline drawing (1/4)



Note: A thermal pad is required on the application board for thermal dissipation. For more information, refer to AN5853.

Note: For more information, refer to the pin description in Table 3. VL53L7CH pin description.

Figure 25. Outline drawing (2/4) - module with liner

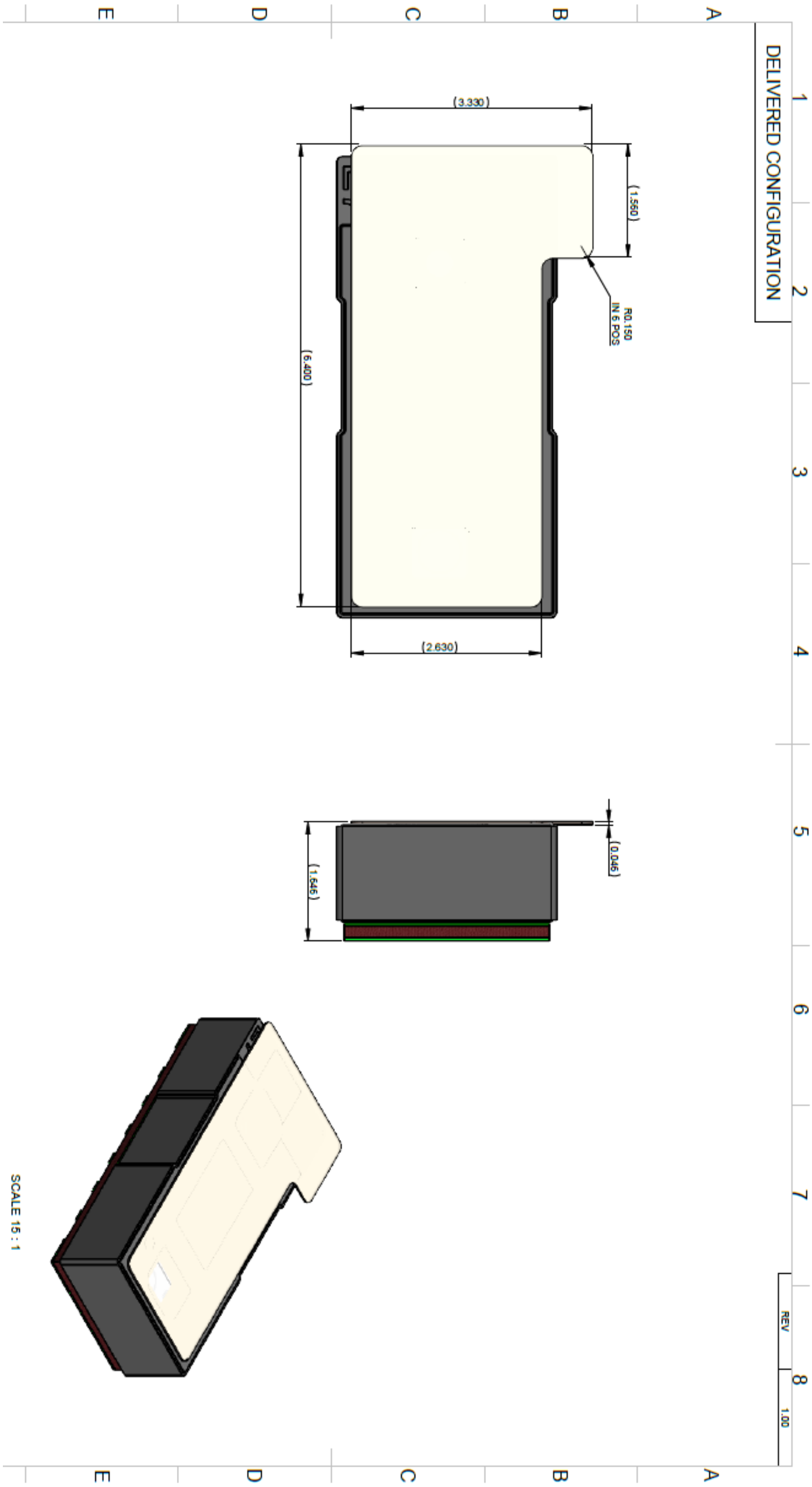
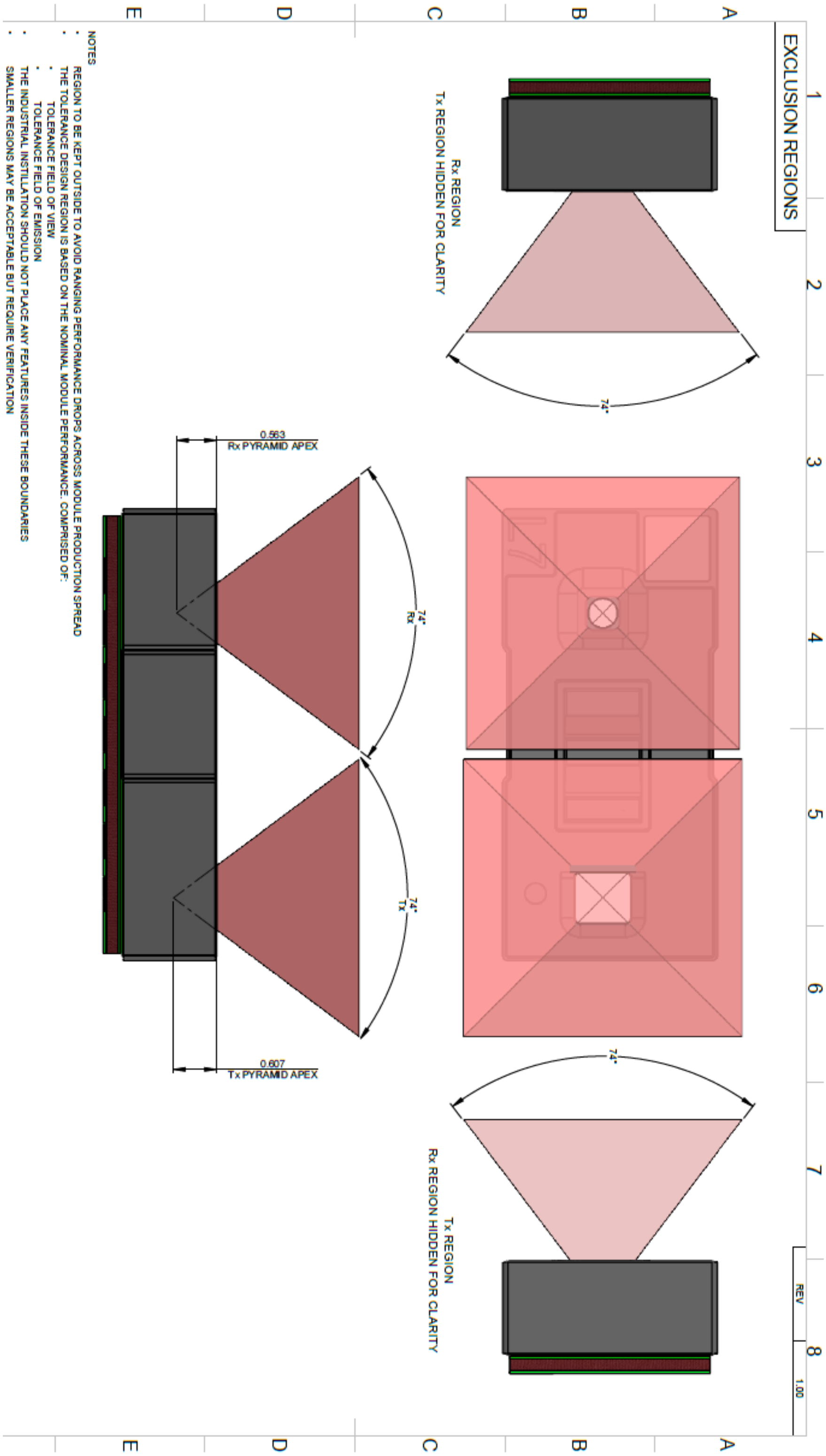


Figure 26. **Outline drawing (3/4) - optical exclusion zones**



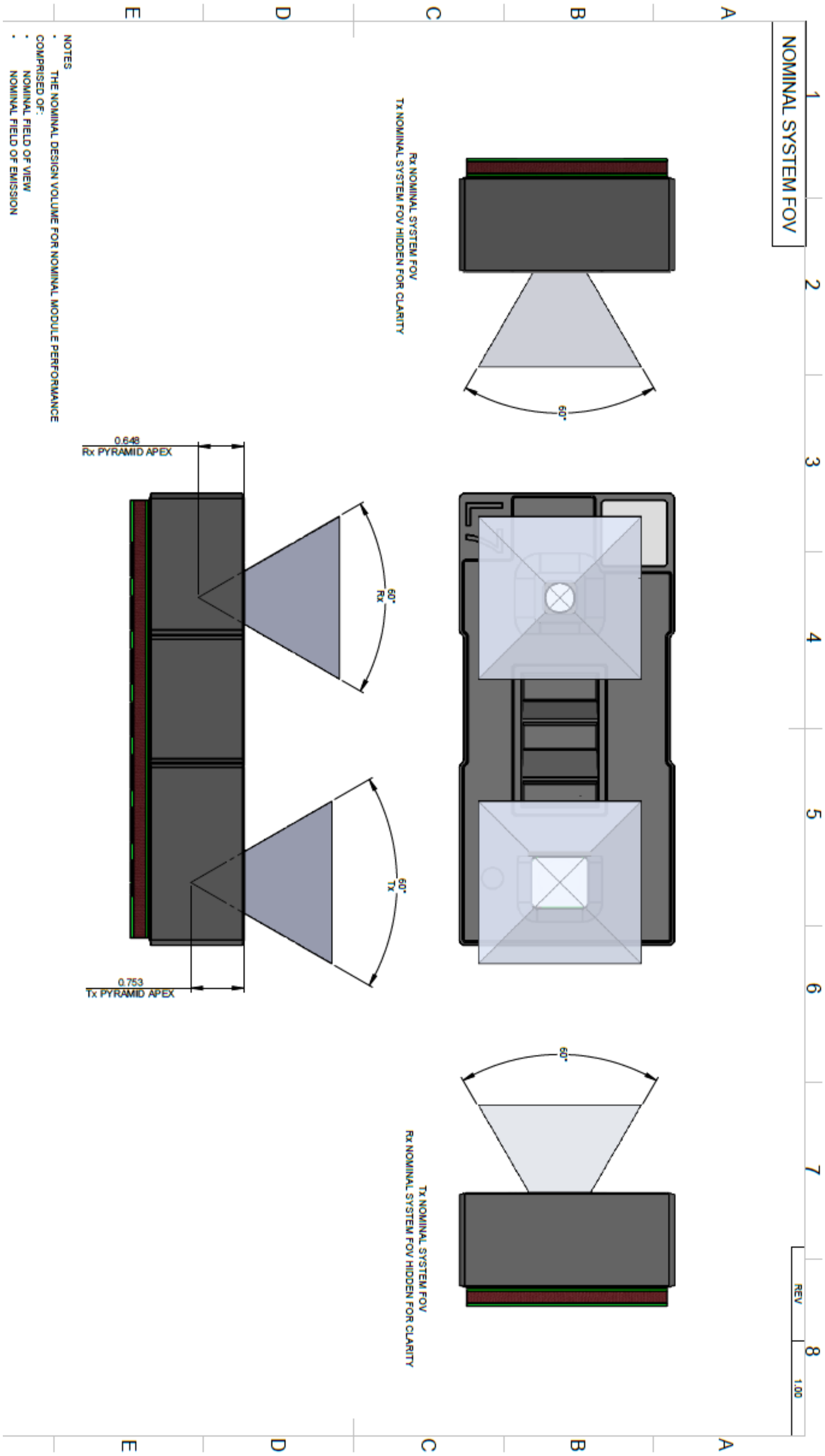


Figure 27. Outline drawing (4/4) - optical system FoV

9 Laser safety considerations

The VL53L7CH contains a laser emitter and corresponding drive circuitry. The laser output is designed to meet Class 1 laser safety limits under all reasonably foreseeable conditions including single faults in compliance with IEC 60825-1:2014.

Do not increase the laser output power by any means. Do not use any optics to focus the laser beam.

Caution: Use of controls or adjustments, or performance of procedures other than those specified herein may result in hazardous radiation exposure.

Figure 28. **Class 1 laser label**

The VL53L7CH complies with

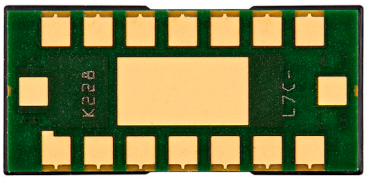
- IEC 60825-1:2014
- 21 CFR 1040.10 and 1040.11 except for conformance with IEC 60825-1:2014 as described in Laser Notice No.56, dated May 8, 2019
- EN 60825-1:2014 including EN 60825-1:2014/A11:2021
- EN 50689:2021 except for the requirement of clause 5 from EN50689 regarding child appealing products. If designing a child appealing product, please contact ST Technical Application Support.

10 Packaging and labeling

10.1 Product marking

See the figure below for the product marking area. The marking is L7C-.

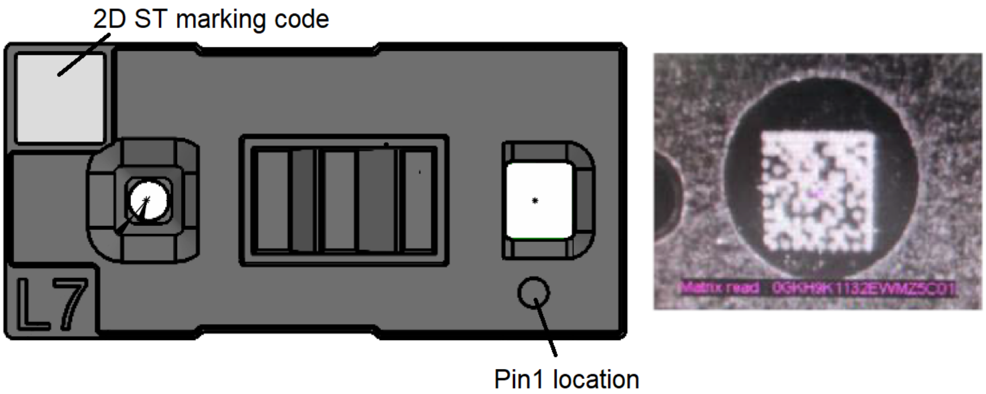
Figure 29. Product marking area



A 2D product marking code is applied on the corner of the module cap as shown in the figure below.

Note: The 2D marking code aligns with pin C7 of the module and is not an indicator of pin 1.

Figure 30. 2D product marking code



10.2 Inner box labeling

The labeling follows the ST standard packing acceptance specification.

The following information is on the inner box label:

- Assembly site
- Sales type
- Quantity
- Trace code
- Marking
- Bulk ID number

10.3 Packing

At customer/subcontractor level, it is recommended to mount the VL53L7CH in a clean environment.

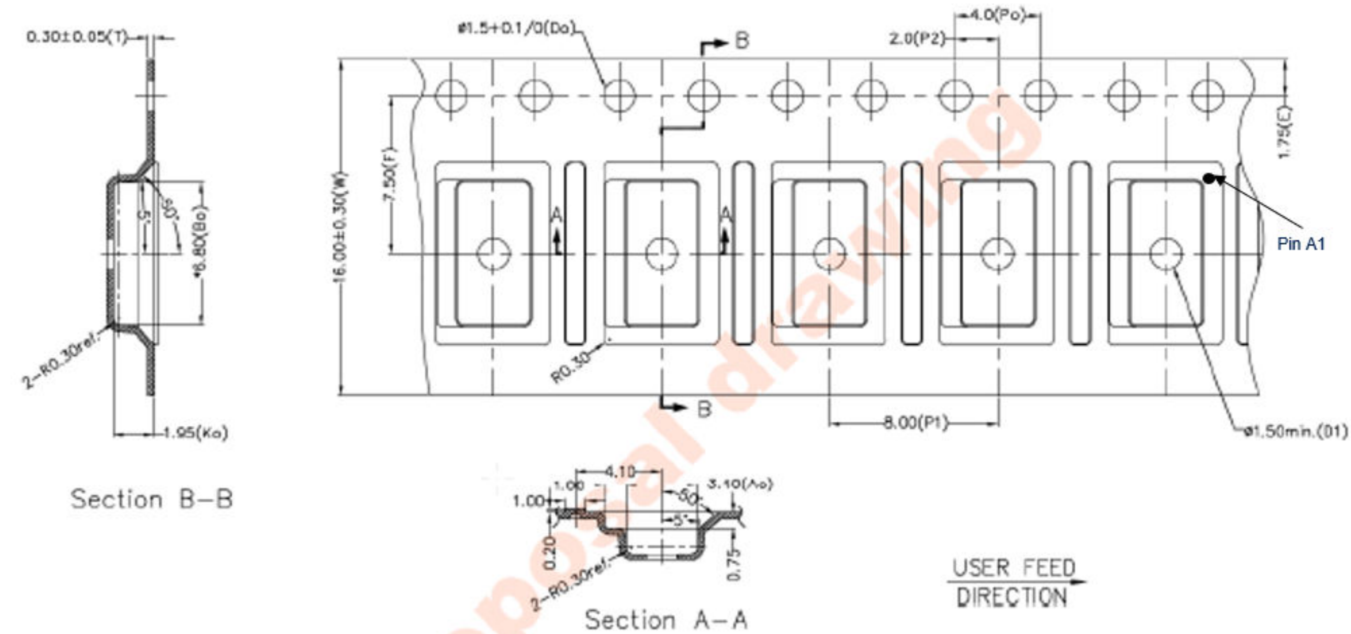
To help avoid any foreign material contamination at final assembly level the modules are shipped in a tape and reel format with a protective liner.

The liner is compliant with reflow at 260°C (as per JEDEC-STD-020E).

Note: The liner must be removed during assembly of the customer device, just before mounting the cover glass.

10.4 Tape outline drawing

Figure 31. VL53L7CH tape outline and reel packaging drawing



No.	Order Code	Description	Color	Product Shipped
1	eCA2017-PC-BLK-L	eC3-EWOK MZ 2.0-16-8-P1-L	Black	

NOTES:

1. MATERIAL:CONDUCTIVE PC(C6)
2. Po/P1 10 PITCHES CUMULATIVE TOLERANCE ON TAPE: ±0.20
3. Ao & Bo MEASUREMENT POINT TO BE 0.3 FROM BOTTOM POCKET.
4. ALLOWABLE CAMBER TO BE 1/100mm, NON-CUMULATIVE OVER 250mm
5. SURFACE RESISTIVITY 10^4 TO 10^11 OHMS/SQ OR
   SURFACE RESISTANCE 10^5 TO 10^11 OHMS
6. UNLESS OTHERWISE SPECIFIED ALL INSIDE RADII SHOULD BE 0.25MAX
7. MOLD TYPE:ROTARY MOLD

10.5 Pb-free solder reflow process

The table and figure below show the recommended and maximum values for the solder profile.

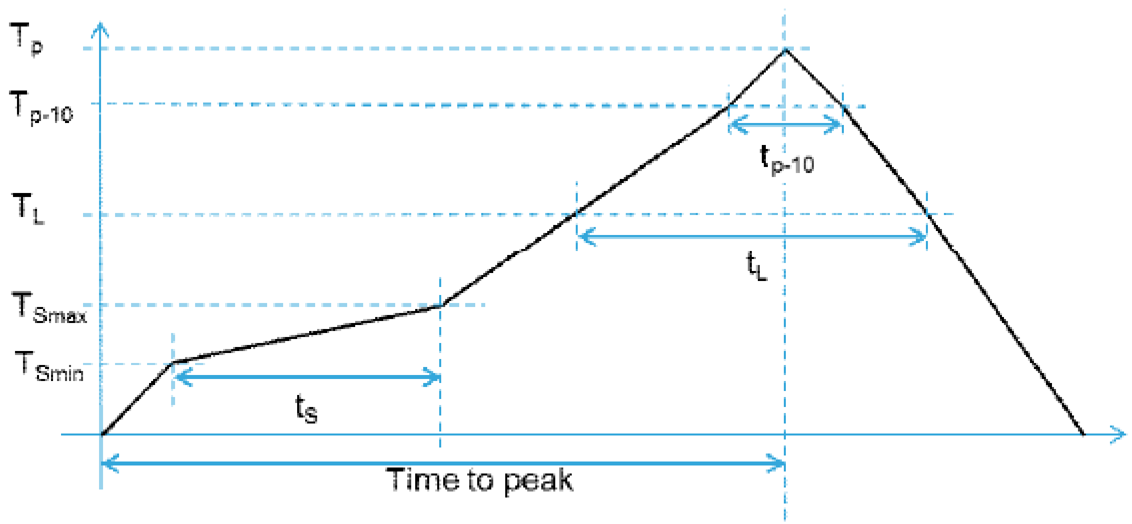
Customers have to tune the reflow profile depending on the PCB, solder paste and material used. We expect customers to follow the “recommended” reflow profile, which is specifically tuned for the VL53L7CH package.

For any reason, if a customer must perform a reflow profile which is different from the “recommended” one (especially peak >240°C), the new profile must be qualified by the customer at their own risk. In any case, the profile has to be within the “maximum” profile limit described in the table below.

Table 26. Recommended solder profile

Parameters	Recommended	Maximum	Units
Minimum temperature (T_S min)	130	150	°C
Maximum temperature (T_S max)	200	200	°C
Time t_s (T_S min to T_S max)	90-110	60-120	s
Temperature (T_L)	217	217	°C
Time (t_L)	55-65	55-65	s
Ramp up	2	3	°C/s
Temperature (T_{p-10})	—	235	°C
Time (t_{p-10})	—	10	s
Ramp up	—	3	°C/s
Peak temperature (T_p)	240	260	°C
Time to peak	300	300	s
Ramp down (peak to T_L)	-4	-6	°C/s

Figure 32. Solder profile



Note: The component should be limited to a maximum of three passes through this solder profile.

Note: As the VL53L7CH package is not sealed, only a dry reflow process should be used (such as convection reflow). Vapor phase reflow is not suitable for this type of optical component.

Note: The VL53L7CH is an optical component and as such, it should be treated carefully. This would typically include using a ‘no-wash’ assembly process.

10.6 Handling and storage precautions

10.6.1 Recommended solder pad dimensions

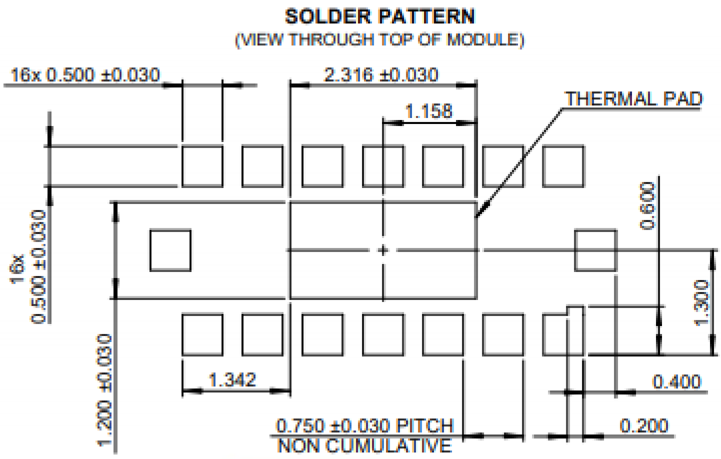


Figure 33. **Recommended solder pattern**

10.6.2 Shock precautions

Sensor modules house numerous internal components that are susceptible to shock damage. If a unit is subject to excessive shock, is dropped on the floor, or a tray/reel of units is dropped on the floor, it must be rejected, even if no apparent damage is visible.

10.6.3 Part handling

Handling must be done with nonmarring ESD safe carbon, plastic, or teflon tweezers. Ranging modules are susceptible to damage or contamination. The customer is advised to use a clean assembly process until a protective cover glass is mounted.

10.6.4 Compression force

A maximum compressive load of 25 N should be applied on the module.

10.6.5 Moisture sensitivity level

Moisture sensitivity is level 3 (MSL) as described in IPC/JEDEC JSTD-020-C.

Note: If devices are stored out of the packaging for more than 168 hours, the devices should be baked before use. The optimum bake recommended is at + 90°C for a minimum of 6 hours.

10.7 Storage temperature conditions

Table 27. **Recommended storage conditions**

Parameter	Min.	Typ.	Max.	Unit
Temperature (storage)	-40	23	90	°C

11 Ordering information

The VL53L7CH is currently available in the formats below. More detailed information is available on request.

Table 28. **Order codes**

Order codes	Package	Packing	Minimum order quantity
VL53L7CHV0GC/1	Optical LGA16 with liner	Tape and reel	3600 pcs

12 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Revision history

Table 29. **Document revision history**

Date	Version	Changes
05-Jun-2023	1	Initial release

Contents

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